



# Exercise: Noise

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# Exercise 1: Noise in Resistors

- Connect a  $1\text{k}\Omega$  resistor (from AnalogLib) on one side to gnd!
- Simulate the voltage noise spectrum on the other side
  - Is it flat?
  - Is the absolute value what you expect?  
Note how the prefixes (e.g. 'a' for Atto) are used...
- Add an ideal low pass filter with corner frequency 10 MHz
  - Use a simple RC and set the 'Generate Noise?' flag of R to 'No'
  - Choose R much larger than  $1\text{k}\Omega$  to not 'load' the 'source'
  - How does the spectrum look like?
  - How much has noise decreased at the corner?
  - Integrate over a large frequency range to get the rms noise
  - Is it what you expect?
- Determine the overall RMS noise ( `totalNoise("noise" nil nil)` )
  - Is it what you calculate?



## Exercise 2: Noise in MOS Transistors



- Instantiate an NMOS and a PMOS of  $W/L = 30\mu\text{m}/0.3\mu\text{m}$
- Apply a fixed drain voltage of, say, 1V
- Find the gate voltages required for drain currents of  $100\mu\text{A}$ 
  - Use a DC sweep
- Determine the transconductance for this operation point
  - Use an AC analysis
  - What  $g_m$  values do you get? Compare NMOS and PMOS.
- Observe the noise current spectra at the drains
  - Set the drain voltage source as *probe instance* to see *currents*
  - You have to run NMOS and PMOS separately
- What are the white noise magnitudes?
  - Do the values roughly match with what you expect from  $g_m$ ?
- Where are the  $1/f$  corners? (Use Log Plot!)
- For one device, increase the current and observe the spectrum



## Exercise 3: Noise in Current Mirror

- Make an 1:1 PMOS current mirror, using the same PMOS as in the previous exercise.
  - (PMOS is better for lower  $1/f$  noise here)
- Load the output with 1V. Inject a current at the input and verify that you get the current at the output
- Plot the noise at the output.
- Now add a decoupling capacitor (to gnd!) to the bias node.
- Plot the noise spectrum for  $C_{\text{dec}} = 1/10/100/\dots$  fF
  - Observe how larger decoupling cuts down the noise at lower frequencies
  - Why is there no added noise at very high frequency ?
  - Check that the 'corner' frequencies for various caps are where you expect them !



## Exercise 4: Charge Amplifier

- Design a charge amplifier followed by a (passive) CR-RC filter with corner frequency  $\tau \sim 1\mu\text{s}$  with input cap of 1 pF.
  - For the amplifier, use a simple NMOS ( $W/L \sim 10\mu/0.3\mu$ ) gain stage with a PMOS current mirror load ( $30\mu/0.3\mu$ ). Decouple the bias node.
  - Bias at  $\sim 100\mu\text{A}$ .
  - Use a feedback capacitor of 100 fF. Put a  $100\text{M}\Omega$  resistor in parallel to set the dc operation point.
  - Implement the filter as passive RCs, with parameterized  $\tau$ . Use vcvs buffering between the stages. You may want to switch off noise in the resistors...
- In a transient simulation, inject a 1fC charge (1V step across a 1fF injection capacitor)
  - Observe the output of preamp / shaper, and the preamp input
  - Is the virtual ground at the input 'ok'?
  - Is the shaper signal as expected (amplitude, peaking)? Vary  $\tau$ !



## Hint for Exercise 4: Nice Filter

- To make the schematic more tidy, you may make a symbol + schematic of a CR-RC filter with a parameter (peaking time, or corner frequency).
- Turn off the noise of the resistors in the filter, so that we can concentrate on the other stuff.



## Exercise 5: Noise in Charge Amplifier

- Perform a noise simulation for  $\tau = 0.5 \mu\text{s}$  and  $5 \mu\text{s}$
  
- For  $\tau = 1 \mu\text{s}$ :
  - Determine the total noise at the shaper output by integration
  - Take the square root to get the RMS (voltage) noise
  - Divide by the signal for one electron to get the ENC
  - What do you get ?
  
- Double  $C_{\text{in}}$  to  $2 \text{ pF}$ 
  - What is the ENC now?
  
- Find out which noise type / contribution dominates your circuit by using Noise Analysis