Low swing differential logic for mixed signal applications

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Overview

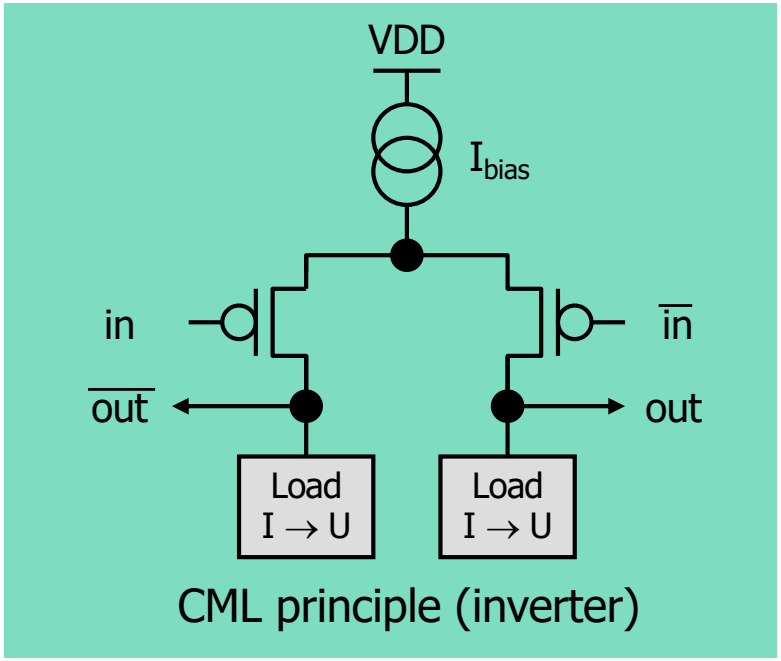
- **Obvious advantages** of low swing, differential **logic** with constant current operation are:
  - **low swing** ⇒ **small** injected cross talk
  - **differential** swings ⇒ **compensation** of spurious injections
  - **constant current** operation (also during transients!) ⇒ **no spikes** on supply and ground (no short circuit current)
- This makes it very attractive for low noise mixed mode FE chips (e.g. pixel chips)

- **Possible drawbacks** are
  - **dc power consumption** may be excessive. However, **speed requirements** in HEP are often **modest** compared to possibilities of DSM chip technologies!
    ☺ It turns out that adequate speed can be achieved with few µW/Gate.
  - **layout area** may be increased due to increased circuit complexity.
    ☺ complex functions can be implemented with less devices than in CMOS.
    ☺ if radhard layout imposes annular NMOS, the small number of NMOS in differential logic is advantageous!
    ☺ the many metal layers available in DSM technologies make routing of twice the number of signals fairly easy.
  - **speed** depends strongly on load capacitance. Selectively adapting the bias current to the load is difficult because this changes the signal levels when standard load circuits are used.
    ☺ a novel load circuit alleviates this problem.

- The **goal of this work** is
  - to design a **prototype chip** in 0.25µm technology using radiation hard layout rules
  - to **study the feasbility** of CML for moderate speed applications
  - in particular **area, speed** and **power dissipation** of typical circuits
  - and to verify operation of a **novel load circuit** which allows easy control of the signal swing.

CML Operation

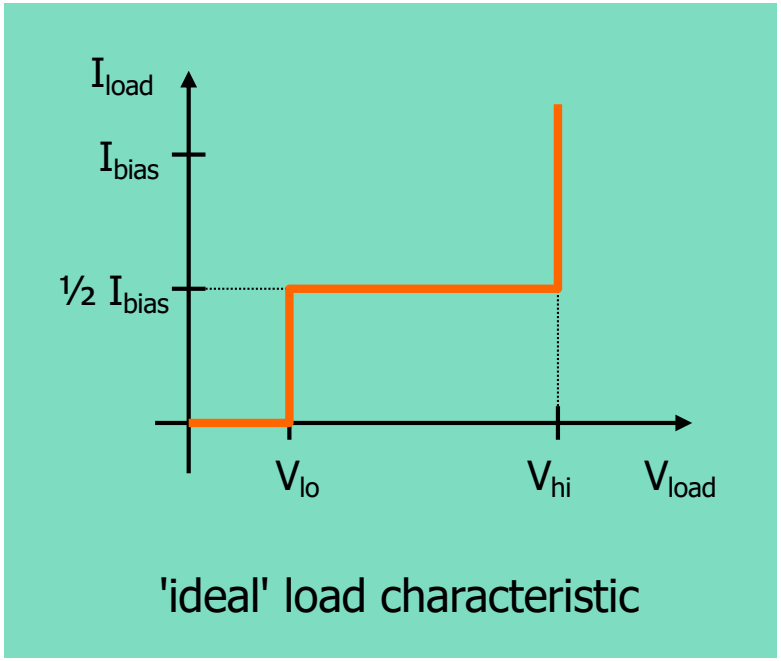
- Differential current mode logic (CML) steers a constant bias current I_{bias} into two load circuits which generate the low voltage swings by $I \rightarrow U$ conversion
- The DC levels must be matched to the common mode input range of the switch block
- Typical loads have linear U/I characteristics or use (pre-biased) diode connected MOS
- Their problem: the swing depends strongly on I_{bias} so that matching to the load capacitance is difficult. This makes circuit design tedious.



CML principle (inverter)

Ideal Load Circuit

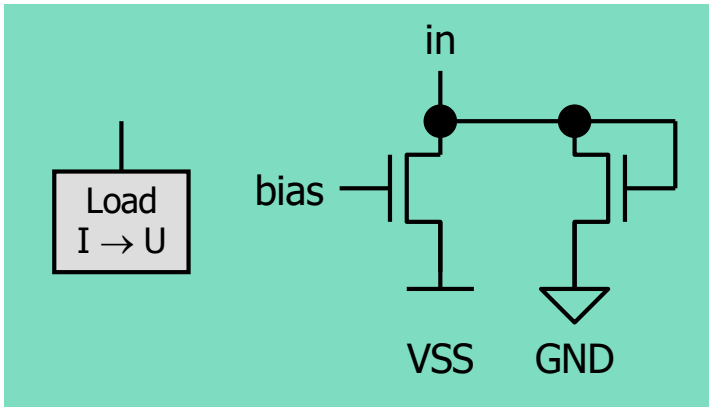
- An **'ideal' load** has the following characteristic:
- The V_{hi}-level is fixed by the maximum possible input voltage to the switch block (~VDD-V_{TP}-V_{DSat})
- The V_{lo}-level is fixed by the voltage swing required to 'fully' switch current in the switch block. For MOS operated in weak inversion, this is below 200mV!
- The plateau at ½ I_{bias} guarantees equal rise and fall times (C_{load} is charged/discharged with ±½ I_{bias})

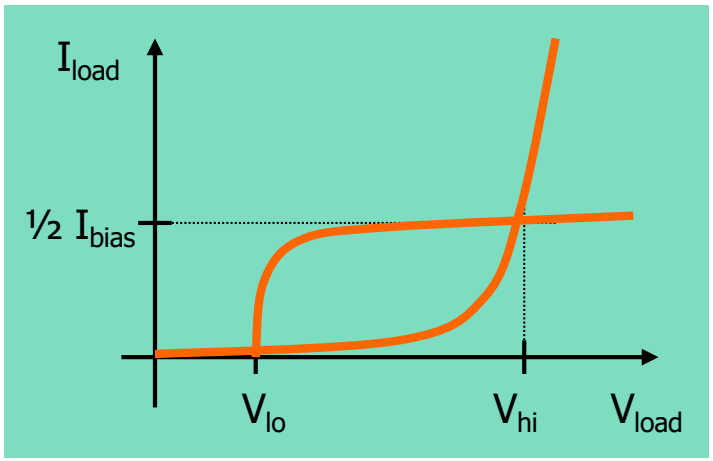


'ideal' load characteristic

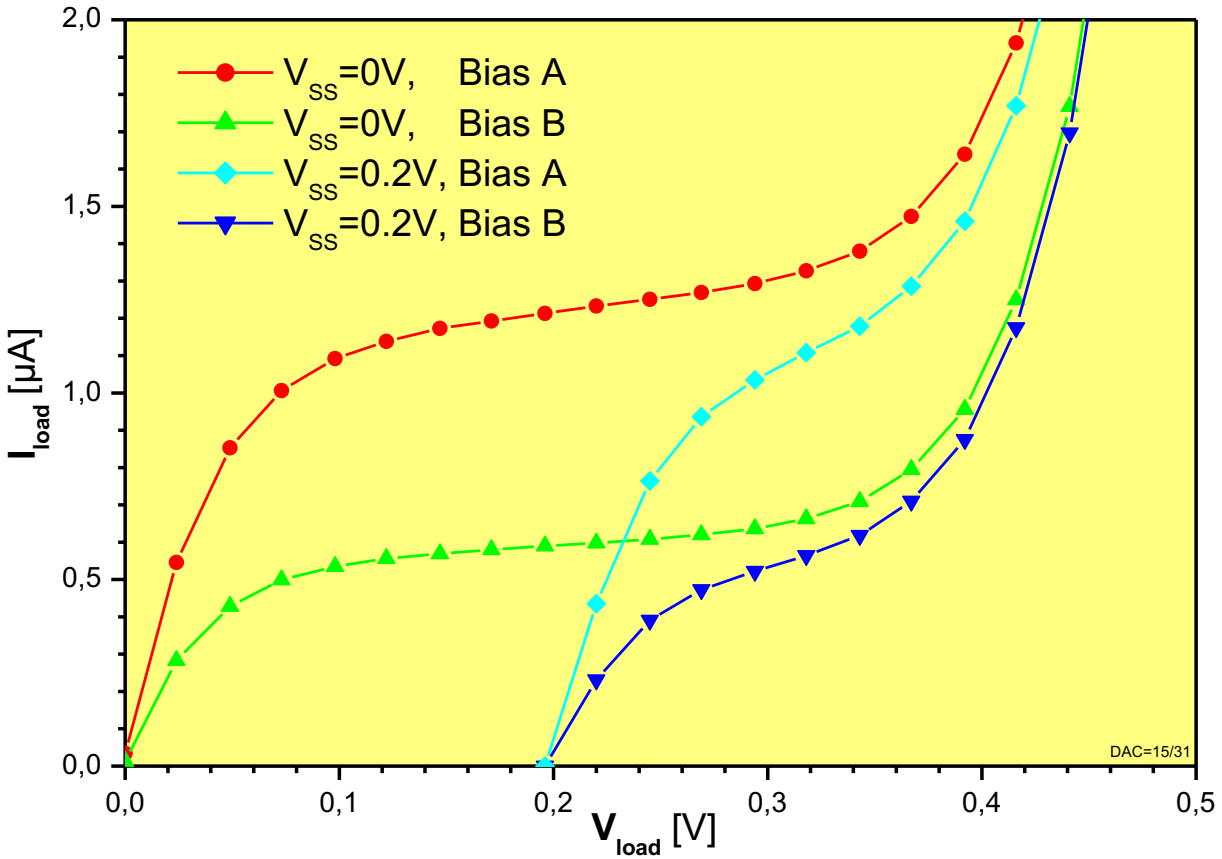
Proposed Load Circuit

- The proposed circuit approximates the 'ideal' characteristic by a parallel connection of:
  - an NMOS operated as a current source with adjustable source voltage VSS
  - a diode connected NMOS (other 'steep' devices like pn-diodes could replace the second NMOS)
- Due to the steep characteristic of the MOS diode (exponential in weak inversion), V_{hi} increases only slowly with I_{bias}
- the differential swing can be easily adjusted through VSS



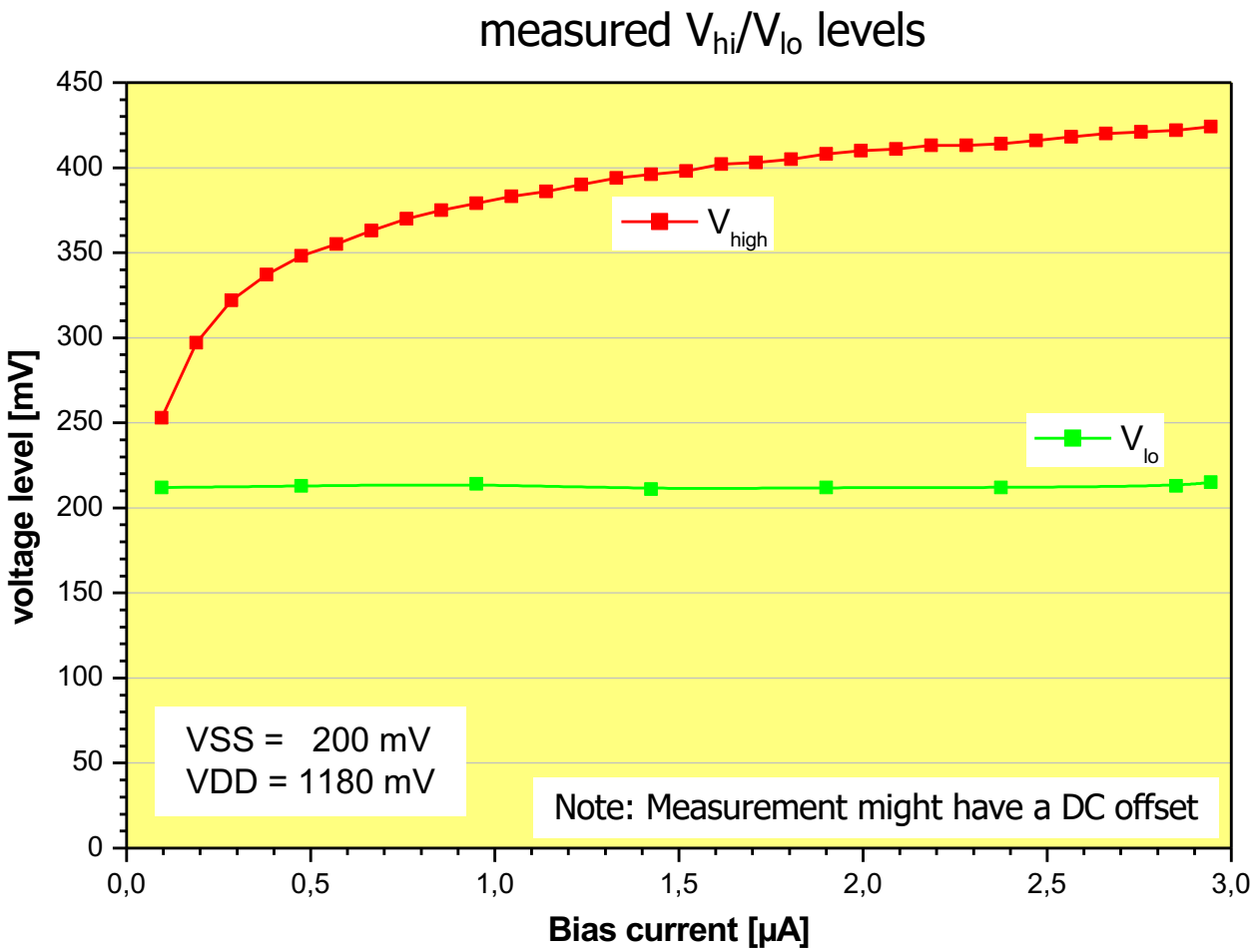


measured load characteristic



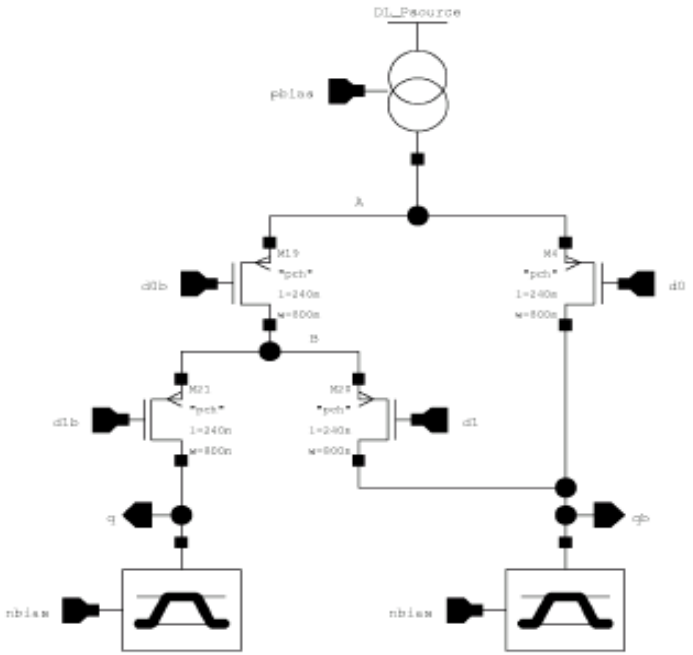
Signal Levels and Supply Voltage

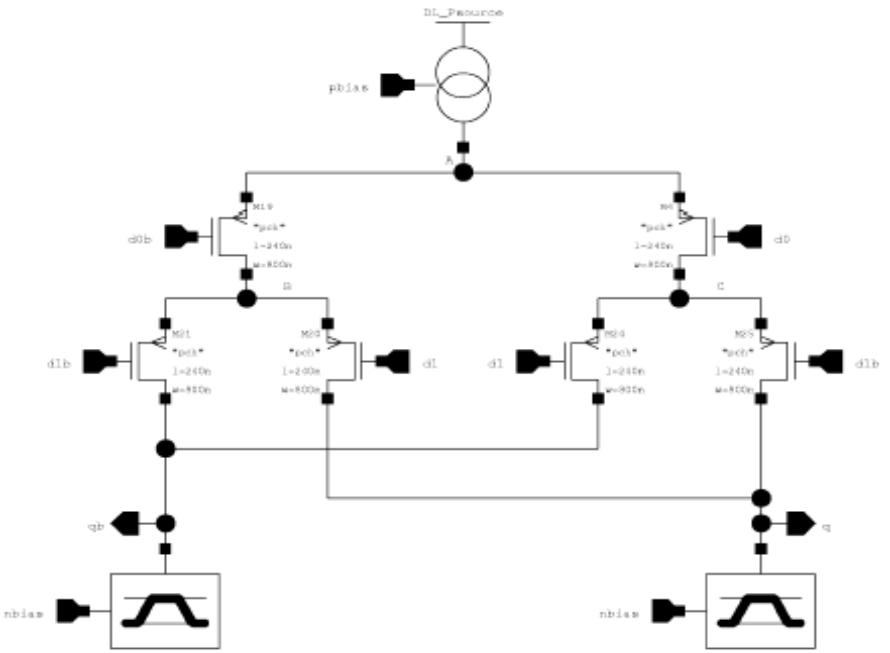
- The **Low level** is constant = **VSS = 0.2V**
- The **High level** depends only logarithmically on I_{bias}: A 10 x higher bias increases the swing by ~ 100mV. A typical value is V_{hi} = ~400mV, i.e. a **swing of ~200mV**.
- Logic can be therefore be operated at a supply voltage of only **VDD = 1.2V**

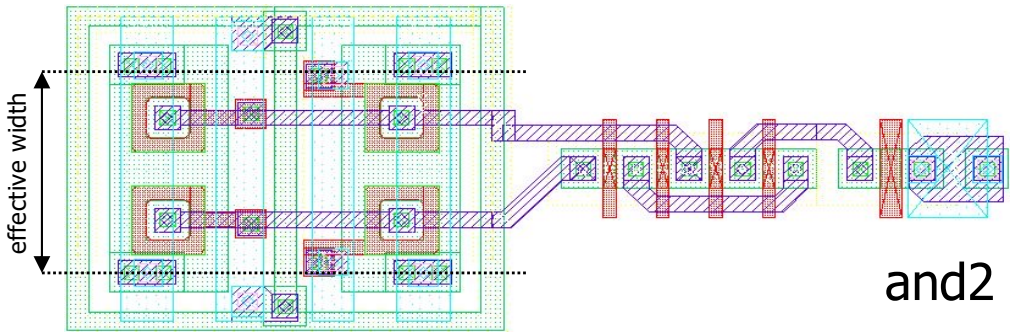


Simple Differential Gates

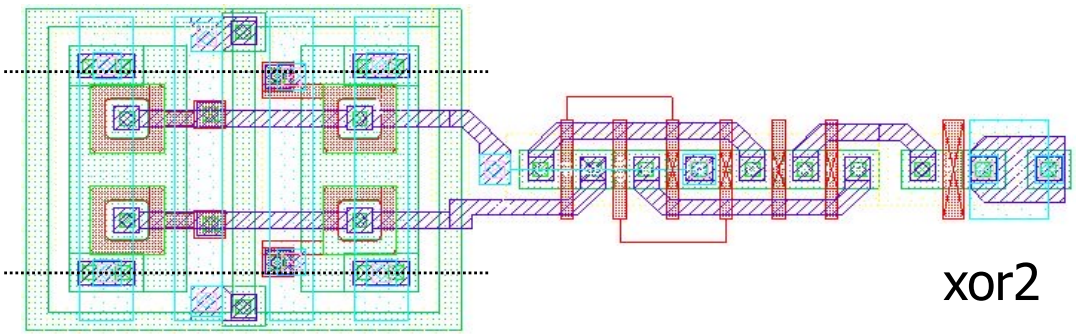
- Only two different gates implement all possible functions of two variables.
  (Inversion of signals is done by swapping differential signals ⇒ OR and AND gates are equivalent)







and2

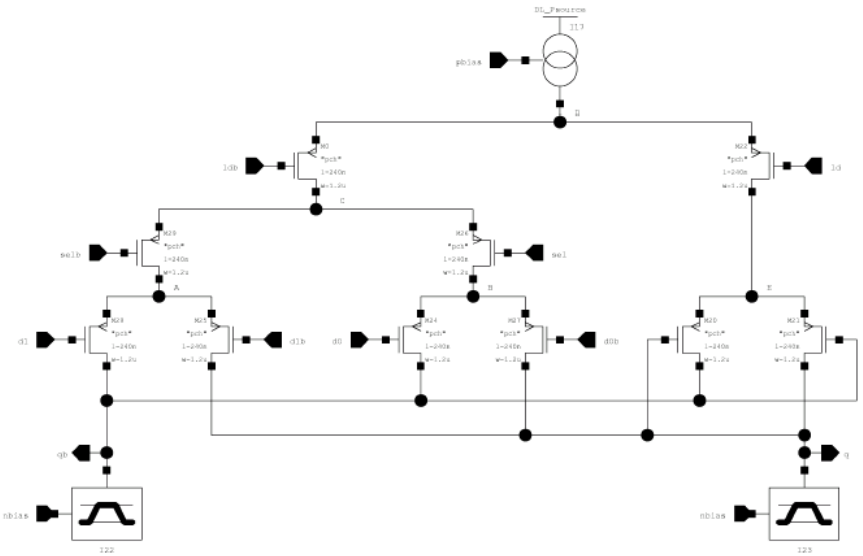


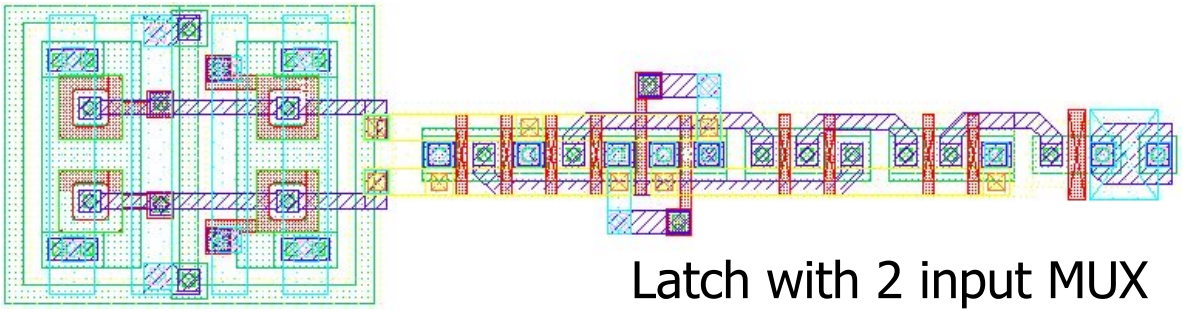
xor2

Complex Differential blocks

- Complex functions can be integrated into one block. This saves transistors for current source and load circuits
- With annular NMOS devices (for radiation hardness), **differential gates can even be smaller than CMOS**!

Function	CMOS		Differential	
	PMOS	NMOS	PMOS	NMOS
and2	2	2	4+1	4
and3	3	3	6+1	4
xor2	5(3)	5(3)	6+1	4
mux2	3	3	6+1	4
latch	4	4	6+1	4
Latch w. input MUX	7	**7**	10+1	**4**



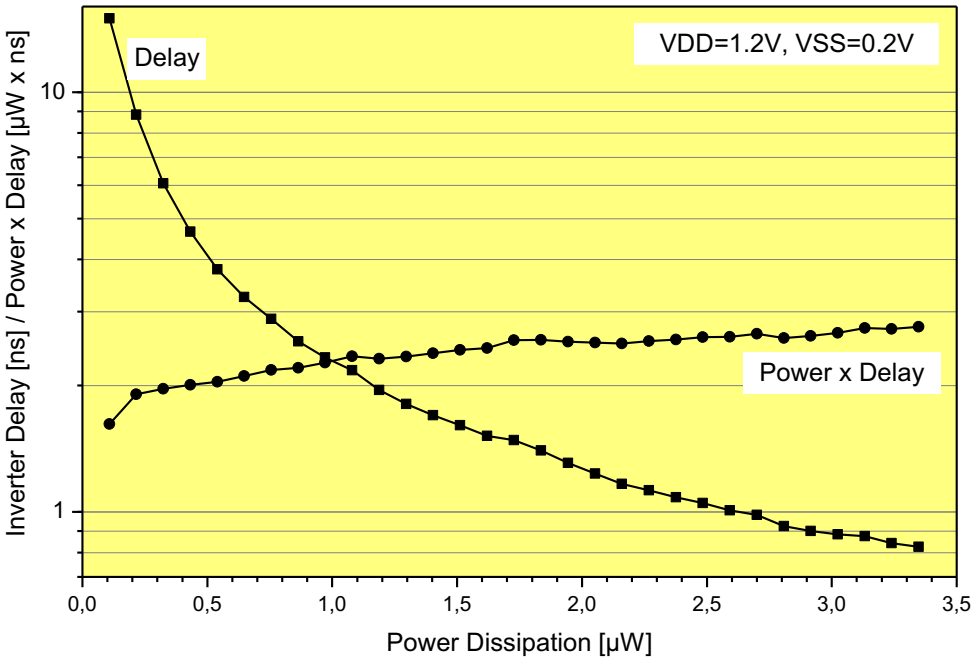


Latch with 2 input MUX

Propagation Delay

- Propagation delay of an inverter has been measured on a test chip.
- Power-Delay product is nearly constant because signal swing is faily independent of I_{bias}.

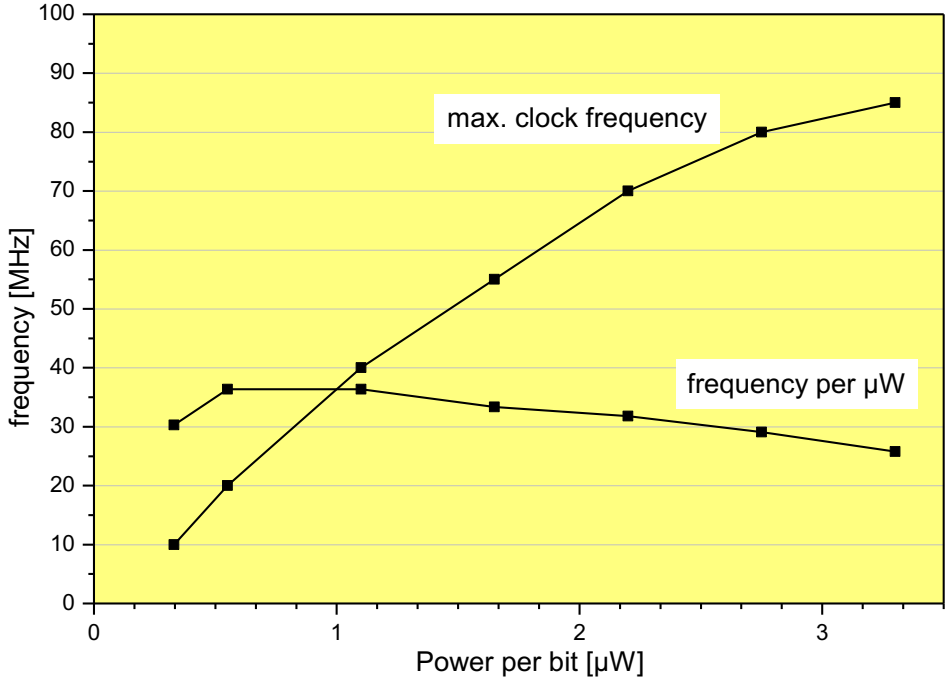
delay and power-delay-product of inverter



Clocking Frequency

- A **8 bit synchronous counter** operates at
  - 8 MHz if operated at 35µW
  - 15 MHz if operated at 81µW
- Maximum clocking frequency of a 32 bit long **shift register** (with parallel load) has been measured on a test chip:

Max. clocking speed of shift register



Design study: 16 bit counter

- A fully differential, fully static 16 bit ripple counter including a parallel readout scheme has been implemented
- Layout area is **50µm** × **50µm** (in a 0.25µm technology using **annular NMOS devices**, using 3M layers)
- Expected size for non-radhard layout is 50µm × 35µm
- The maximum clocking speed depends on the dc power consumption
- A counter operated at a **~6.5µW** operates up to **20 MHz**
- If it disspiates **~35µW**, it operates up to **80 MHz**