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Exercise:
Fast Logic

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Motivation

- We want to explore methods to make fast logic
- We will concentrate on the inverter

- We also try to control the speed of an inverter for later use in a PLL or DLL oscillator

CMOS

- If we simulate just one inverter
  - We may drive it ‘too good’ with a spice source (fast rise)
  - It is not so easy to ‘read’ the delay

- Therefore:
  - Make a chain of (10 or so) CMOS inverters. Use WN for the NMOS, k WN for the PMOS
  - Inject a step
  - See when it passes stage i (after rise/fall has stabilized)
  - See when it passes stage j
  - Calculate the delay.

- Vary WN, k, supply voltage
- Add a second inverter to ‘look at the signal’ at every stage. Speed now?

CMOS with variable delay

- 'Invent' methods to be able to change the delay with a control voltage.
  - For 'full speed', inverters should still be fast

Differential Logic

- Make a differential inverter with
  - An NMOS current source. Dimension the MOS so that we can put up to 1mA…
  - An NMOS differential pair
  - Resistors as loads.
- Start with 100uA
  - How much voltage swing do you need to switch fully?
  - Chose the resistor to get 2x this swing or so
  - What common mode voltage is possible?
- Make a chain as before
  - Use a common current mirror to generate VBiasN of the current source
  - How fast is this?
- Now increase the current
  - What happens?

Differential Logic with PMOS linear load

- We want to replace the resistors by PMOS in the linear region
  - Remember that we need to have a certain resistance
  - Linear region must be 'wide enough'
  - Try to find a good size and gate voltage VbiasP
- If we change VbiasN, we also need to change VBiasP
  - Invent a circuit which 'finds' VBiasP so that the swing is a given voltage (ΔP = 300mV or so) for any VbiasN
  - Hint: Compare the voltage swing you get in a 'test circuit' with ΔP and regulate VBiasP. You can use a vcvs for now.
- Check that swing is now (more or less) independent of VbiasN
- How does speed change?

Differential Logic with NMOS Load

- Use a diode connected NMOS as a load
  - What are the voltage levels if you operate the circuit fast?
  - What if you stop?
  - How could you ‘cure’ this problem?

- Connect the gates of the NMOS loads to an auxiliary voltage.
  - What changes?

Inductive Peaking

- Connect the gates of the NMOS loads to the auxiliary voltage (which can be VDD) though a high (MΩ) resistor.
  - Any change?
- (I may give some dimensions and currents here…)
- Try to calculate the input impedance of the NMOS load taking into account Cgs, Cgd, gm and Rg
- Implement the high resistor with a PMOS
- Can you tune the circuit to be faster than before (at the same NMOS bias current)?