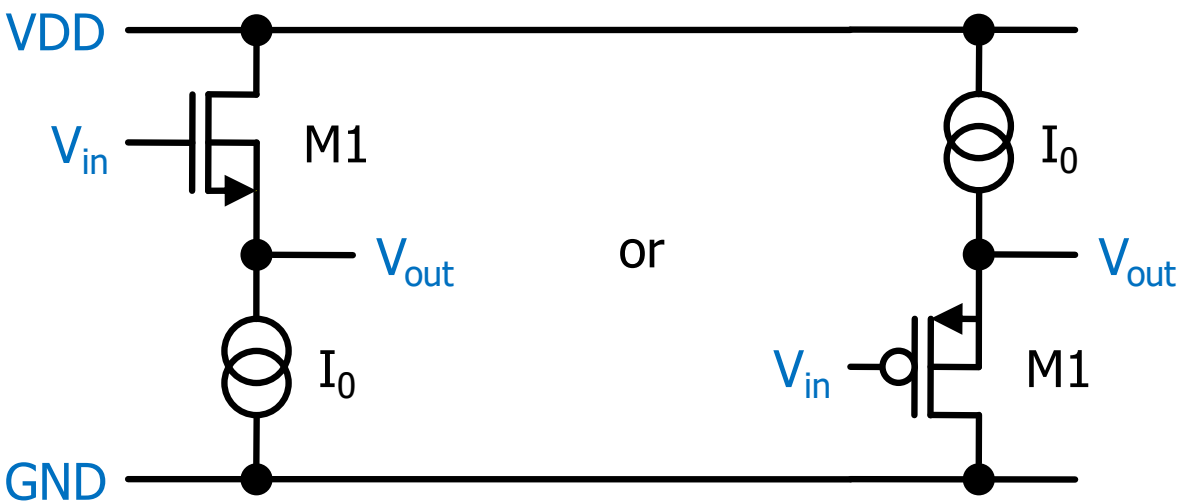
Source Follower and Differential Pair

The Source Follower (Common Drain Stage, SF)

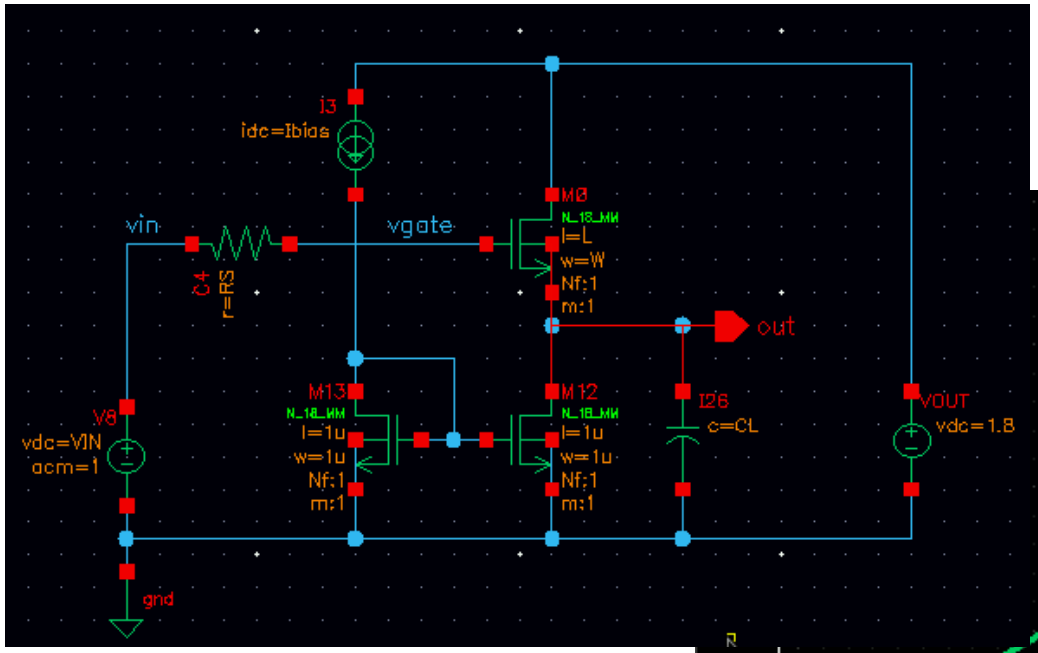
- Current source I_0 pulls a constant current through the MOS
- This fixes V_{GS} of M1 (to V_T + Sqrt(...))
- Therefore, $V_{in} - V_{out} = V_{GS}$ is *nearly* constant (see later)
- The small signal gain is close to 1

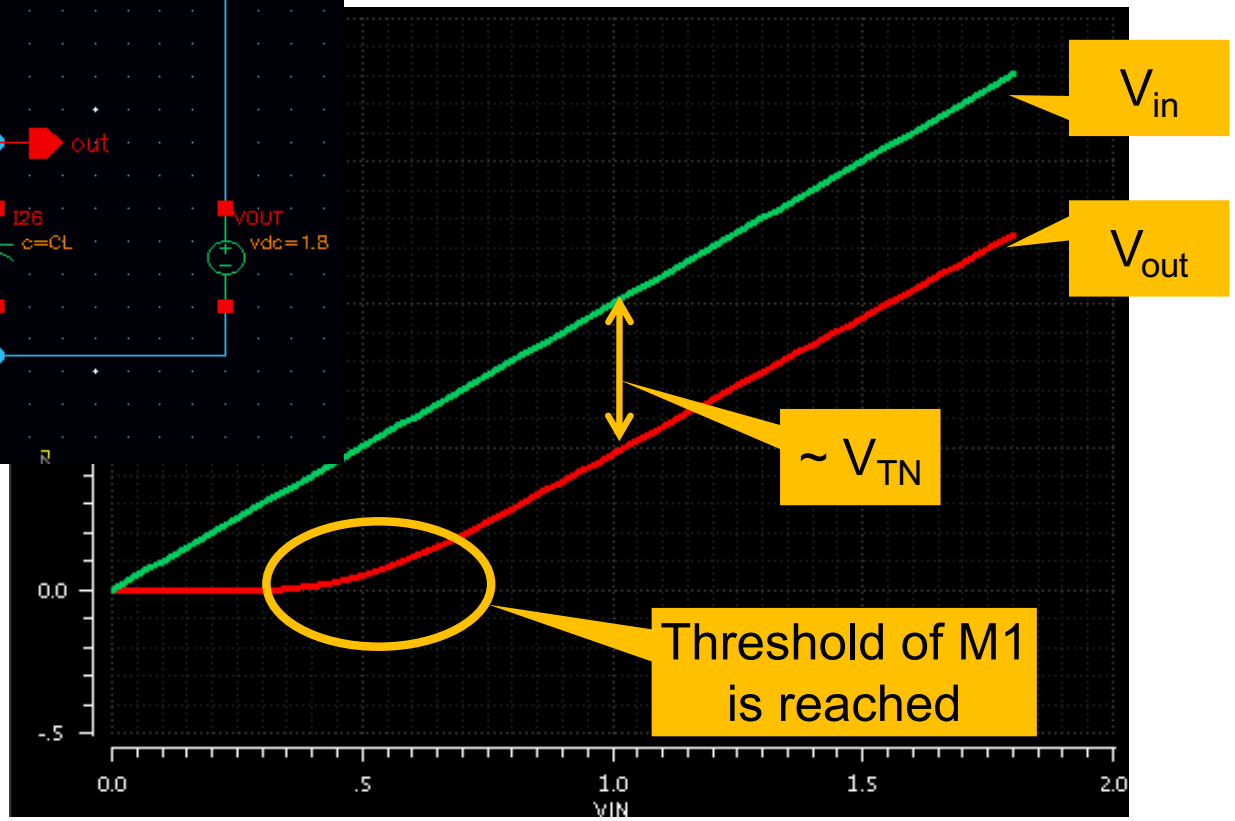
$$V_{out} \sim V_{in} - \text{constant} \rightarrow v_{out} \sim v_{in} \rightarrow g = v_{out}/v_{in} \sim 1$$



Simulation

- NMOS Source Follower with NMOS current source:
  - Starts to works when Vin > $V_{T,NMOS}$ + $V_{DSat,Source}$

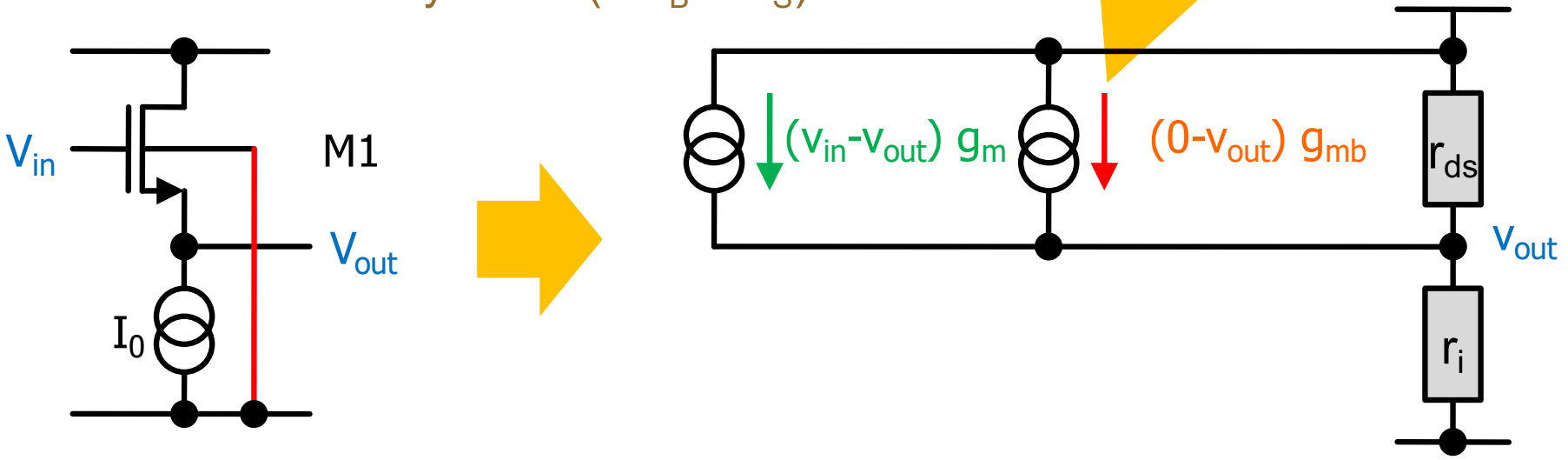




Real Source Follower (Here *with* substrate effect)

- In reality, we must consider
  - r_{ds} of M1 and of current source
  - body effect (if $V_B \neq V_S$)

body effect (if body = ground):
$i = v_{BS}\, g_{mb}$



- gain = $\frac{gm\ rds\ ri}{rds + ri + gm\ rds\ ri + gmb\ rds\ ri} = \frac{gm}{gds + gi + gm + gmb} \sim \frac{gm}{gm + gmb + gds}$

  with $g_{ds} = 1 / r_{ds}$, $g_i = 1/r_i$ and $g_{ds} \ll g_m$...

- Gain is *always* ≤ 1. With $g_{mb} = (n-1)\, g_m$, gain ~ 1/n ~ 0.7

Source Follower with g=1 ?

- From $g = \frac{gm}{gds + gi + gm + gmb}$ we see that we approach g=1 with

  - gmb = 0 → connect bulk an source of M1. This is often not possible for NMOS (bulk = substrate = ground)
  - gi = 0 → Make a good current source:
    - long MOS
    - Cascode, …

    This will lead to higher V_{DSat} so that SF works ‚later'
  - gds = 0 → Hard.
    - Longer MOS helps, but gm suffers (ratio does not increase quickly, speed suffers)
    - Cascode not possible because we change source!

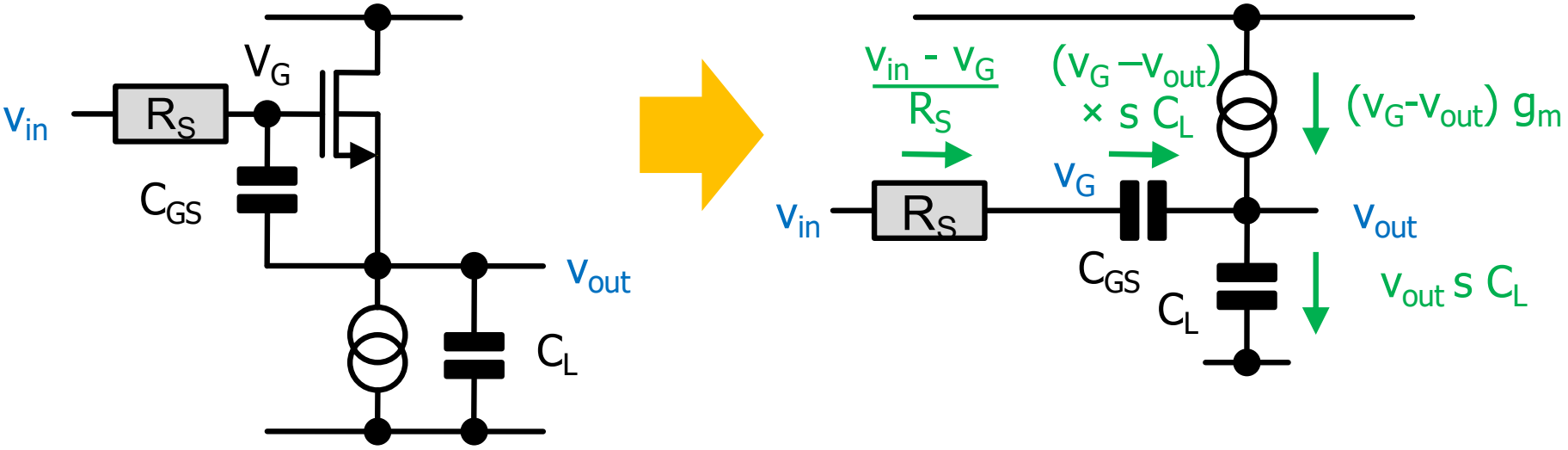
- Reaching an *exact* gain of 1 is not really possible!

- Obvious: If a SF is loaded by a *resistive* load, gain drops!

Advanced: Source Follower with finite source imp.

For instance a gain stage

- Consider the case when the SF is driven by a ‚high impedance' source (with output resistance R_S):
  - Take into account the Gate-Source cap. C_{GS} and output cap. C_L
  - neglect output impedances and g_{mb} for simplicity...



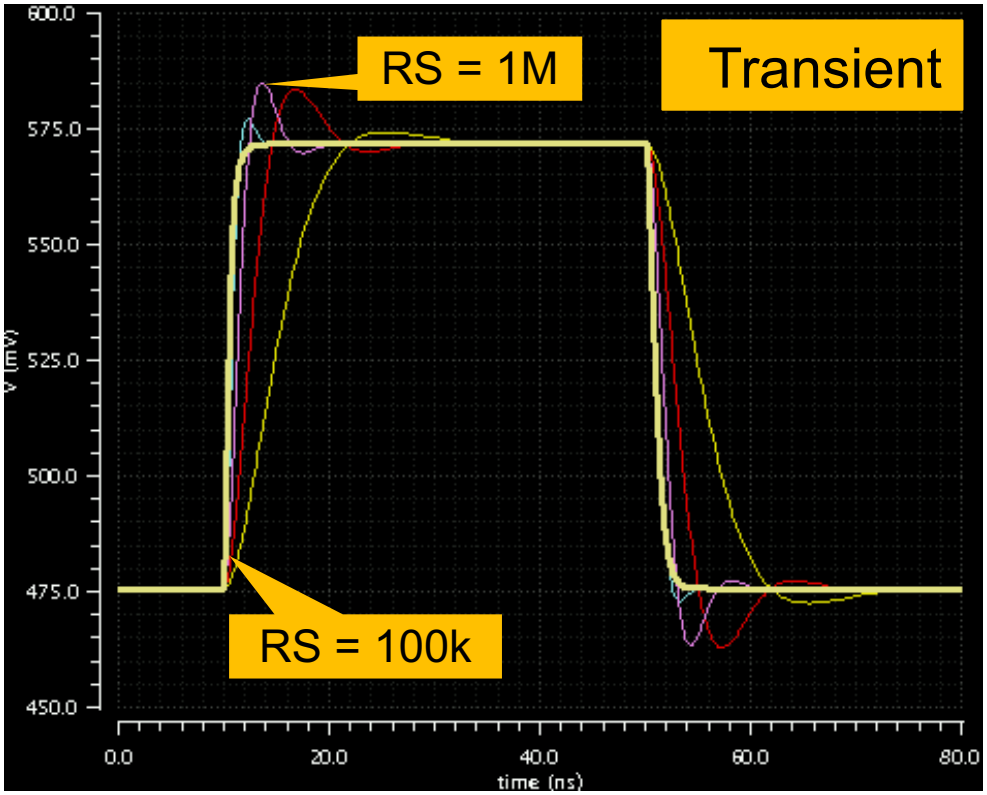
- The transfer function has *two* poles:

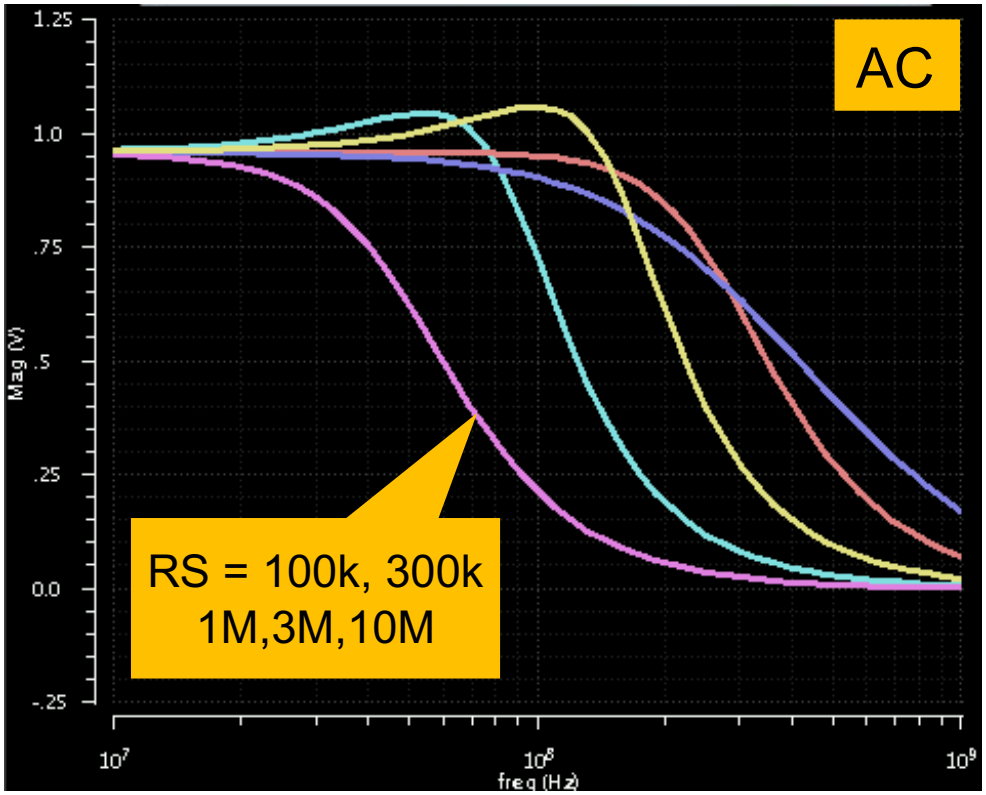
$$\frac{gm + Cgs\ s}{gm + s\,(Cgs + CL + Cgs\ CL\ rs\ s)}$$

- There is an *Overshoot* as soon as $R_S > \frac{(Cgs + CL)^2}{4\ Cgs\ CL\ gm}$

Simulation

- 180nm Technology, W/L = 1µ/0.18µ, C_L = 100fF, I_{bias} = 10µA

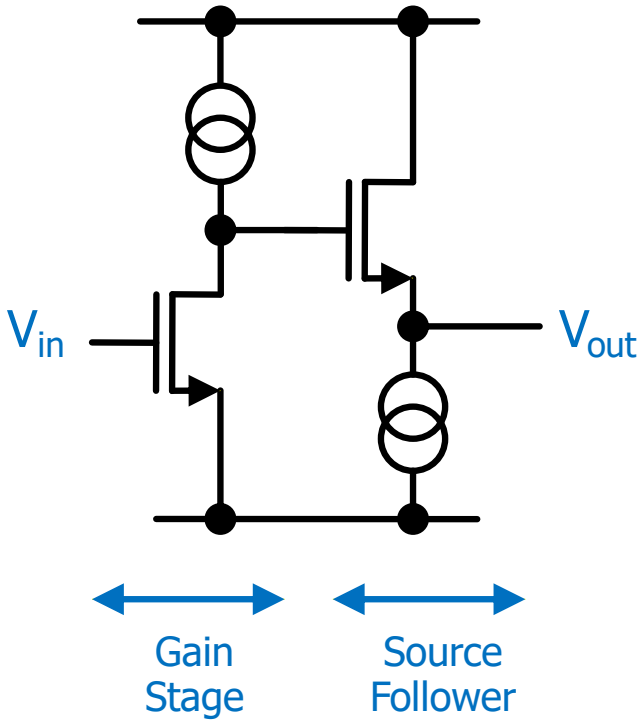




- Therefore remember:
  Source Followers driving capacitive loads are ***dangerous***!

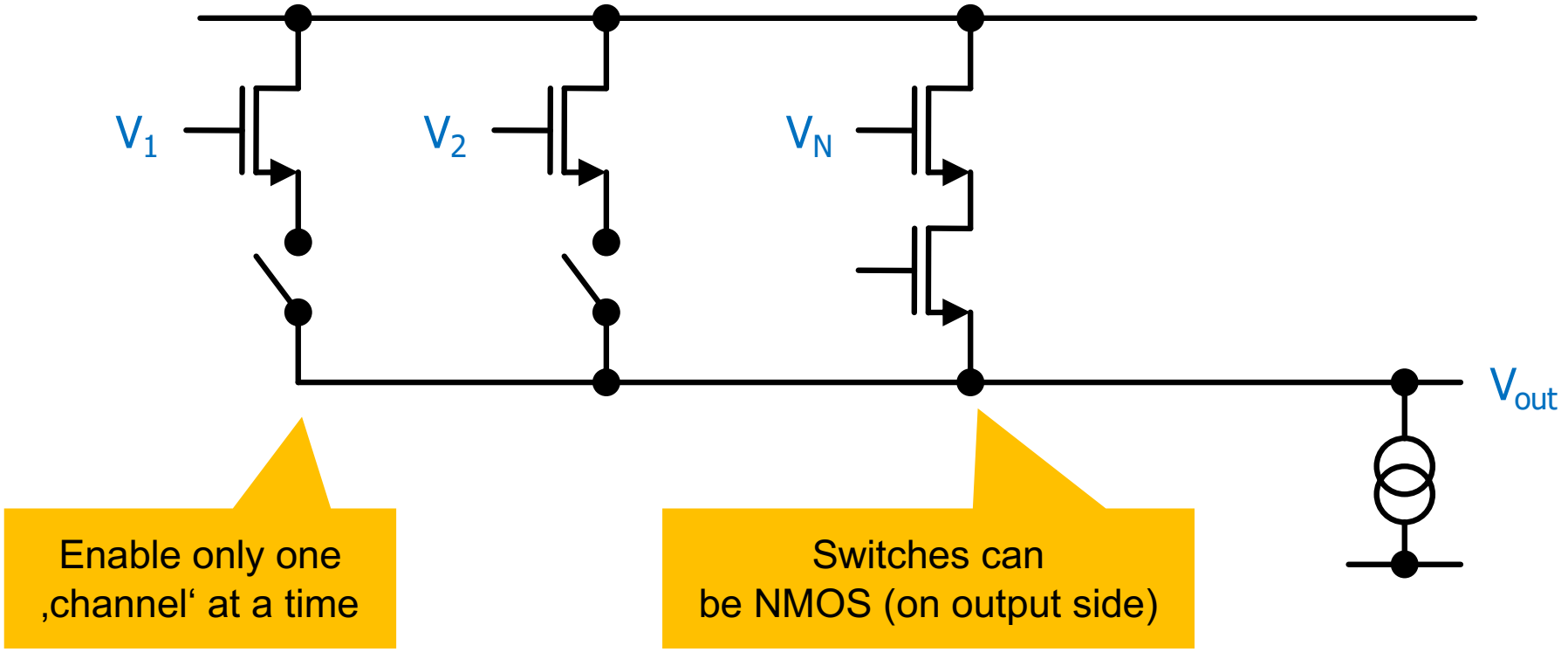
What for?

- The Source Follower has a low output impedance ($1/g_m$)
- It can ‘drive’ low-impedance loads
- Gain drops ‘only a bit’
  - (gain of a gain stage drops ‘a lot’ with resistive loads)
- Often used in combination with a gain stage:



Special Application

- SF be used to ‚send' a voltage
- Multiple Source Followers can be combined:



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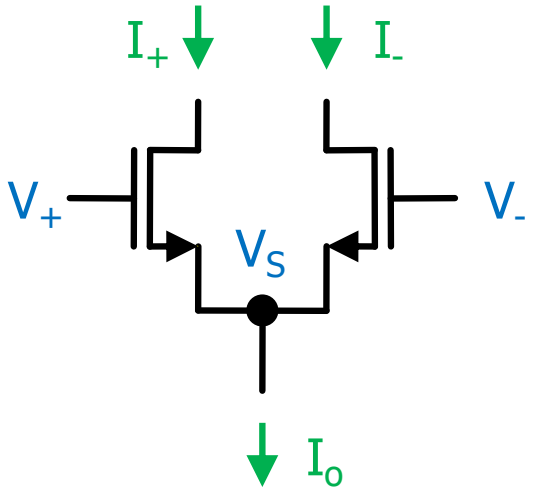
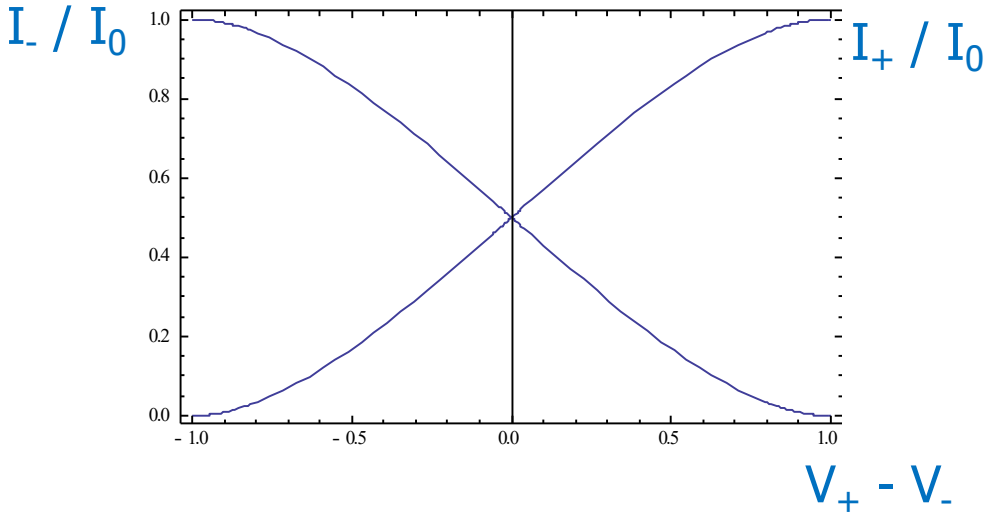
THE DIFFERENTIAL PAIR

The (Differential) Pair

- Very often, the *difference* of voltages must be amplified
- The basic circuit are two MOS with ***connected sources***:





- Assume $V_+ = V_-$
  - → $V_{GS,left} = V_{GS,right}$ → $I_+ = I_- = I_0 / 2$
- Assume $V_+ > V_-$
  - → $V_{GS,left} > V_{GS,right}$
  - → $I_+ > I_-$
- Assume $V_+ \gg V_-$ → $I_+ \sim I_o$, $I_- \sim 0$

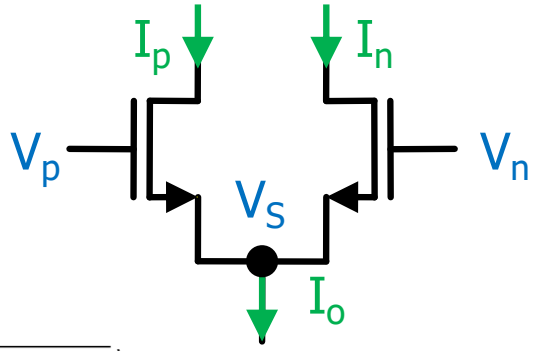
What is V_S ?

- V_S is (roughly) one threshold voltage below the ***higher*** input voltage
- It is often called the 'tail' voltage V_{tail}.
- The pair only works for input voltages > V_{TH}
- The tail current is normally provided by a current source which needs additional (saturation) voltage headroom

The Switching Voltage in ***Strong*** Inversion

- We have `ID[VGS_] = β (VGS - VTH)^2;` with $\beta = K/2\ W/L$
- We have 3 equations for 3 unknowns (I_P, I_N, V_S):

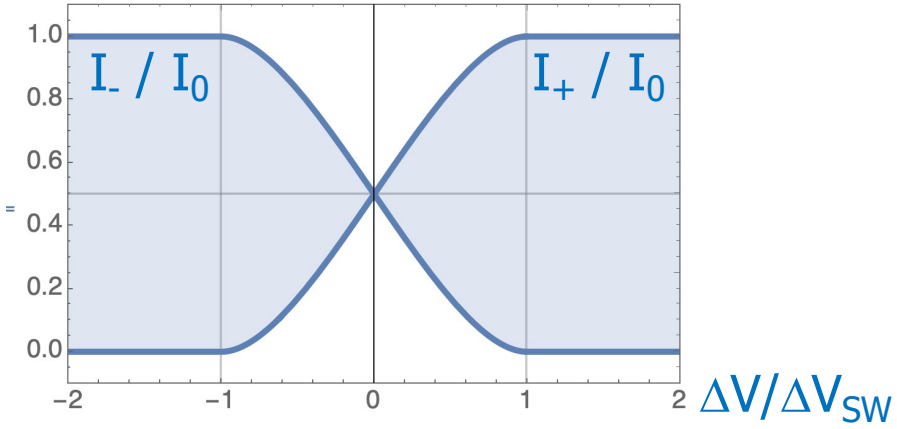
```
IP == ID[VP - VS];
IN == ID[VN - VS];
IP + IN == I0;
```



- We get IP = $\frac{1}{2}\left(I0 + \sqrt{\beta\,\Delta V^2\left(2\,I0 - \beta\,\Delta V^2\right)}\right)$ with $\Delta V = V_P - V_N$

- We switch ***completely*** for

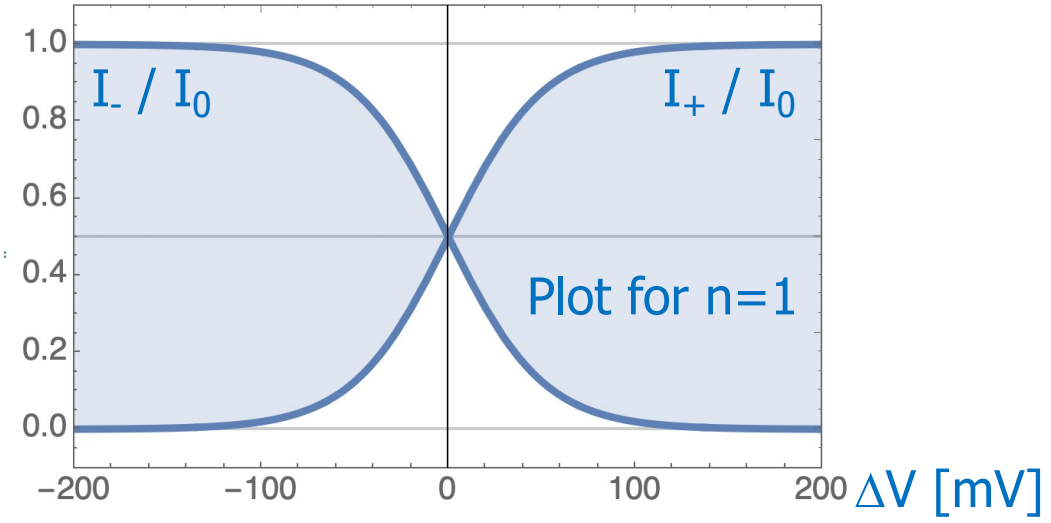
$$\Delta V_{SW} = \frac{\sqrt{I0}}{\sqrt{\beta}}$$



- Conclusion: In *strong inversion*, pair can be *fully* switched!

The Switching Voltage in ***Weak*** Inversion

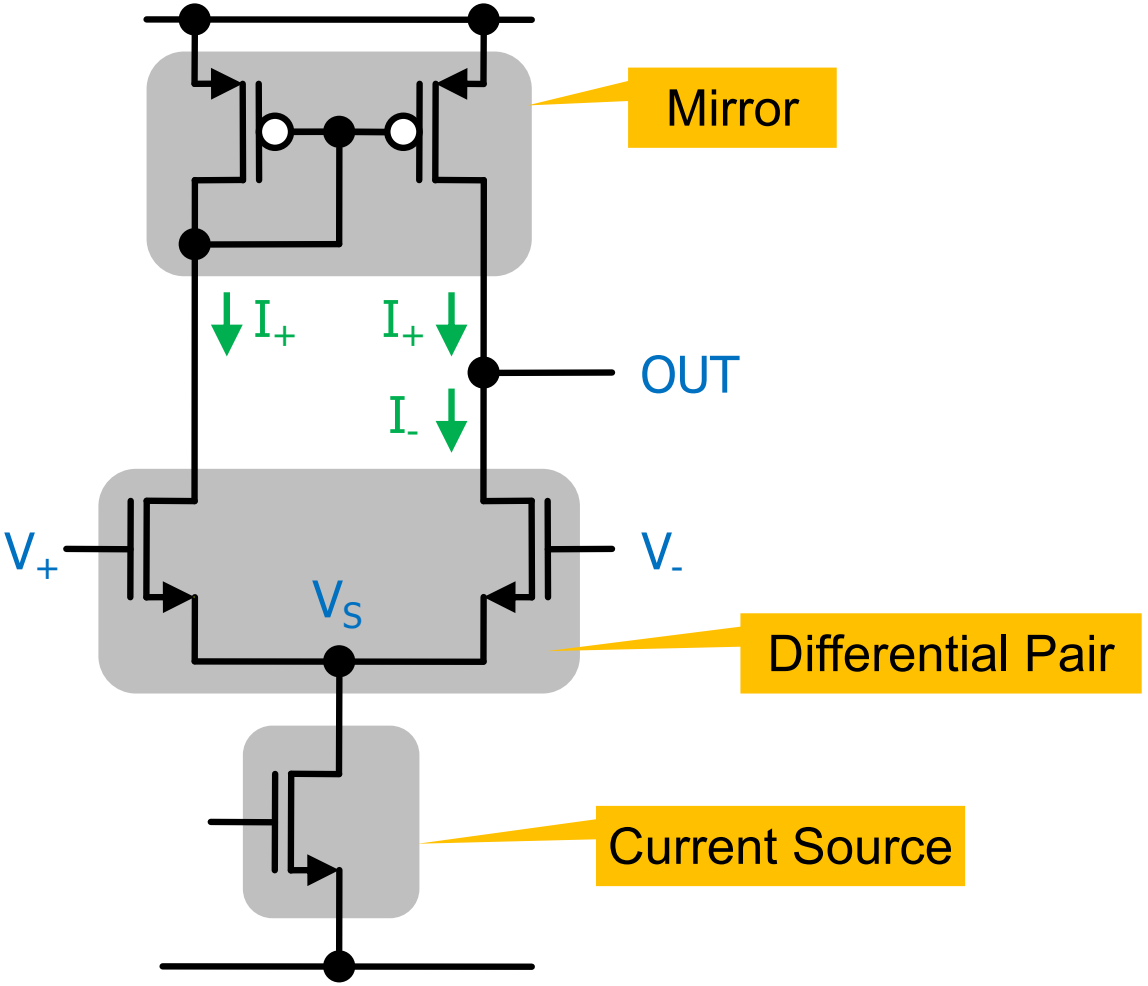
- We have $ID[VGS\_] = \beta \, Exp\left[\frac{VGS}{n\,UT}\right];$
- We get IP = $\frac{I0}{1 + e^{\frac{\Delta V}{n\,UT}}}$ with $\Delta V = V_P - V_N$ and UT = 25.6 mV
- We switch in a few UT, but ***never*** switch 'really' completely



- Conclusion: In *weak inversion*, pair switches at *small voltages*, but never fully!

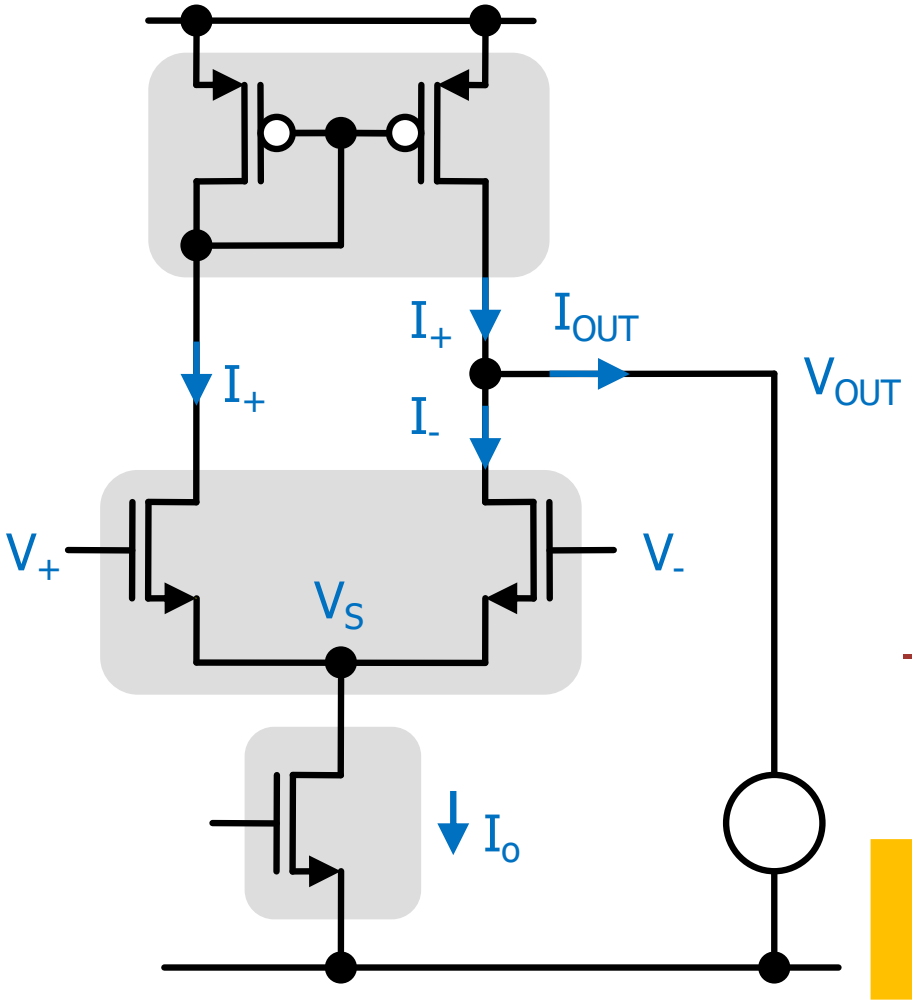
The Differential Amplifier

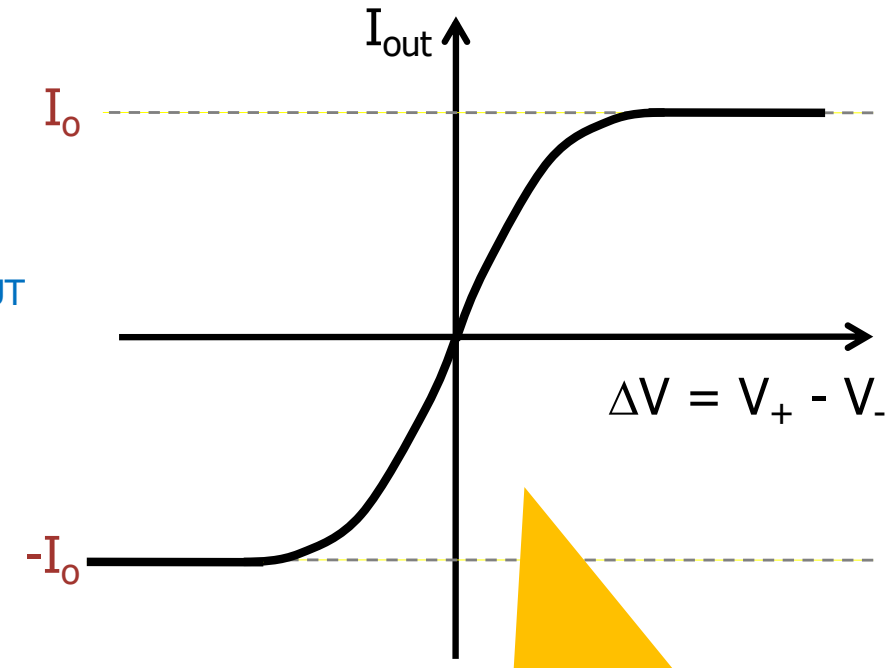
- One ‘output’ current is often mirrored and added to the other:



Output *Current* of the Differential Amplifier

- If the output voltage is *fixed*, the *output current* is just $I_+ - I_-$
- The circuit is a ‚*Transconductor*' (it converts $\Delta U \rightarrow I$)

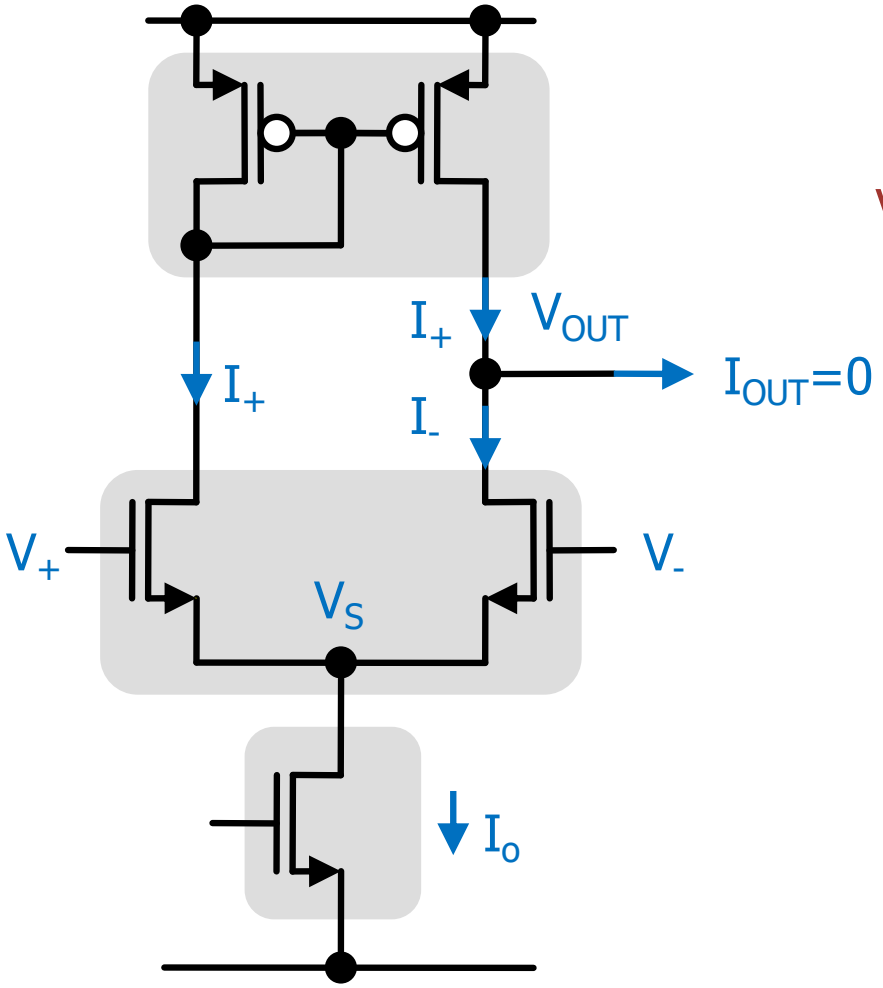


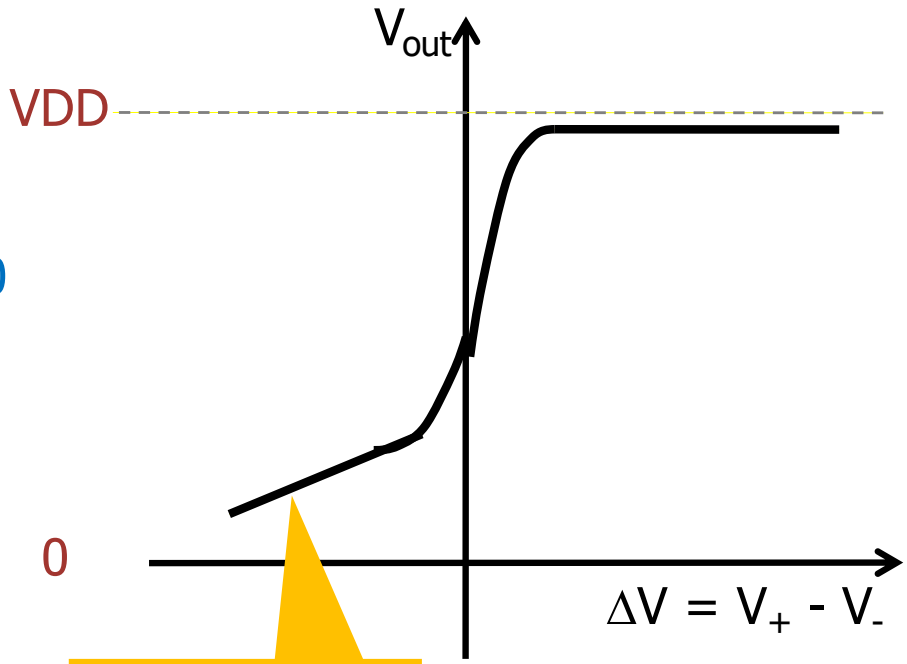


This only works if the V_{OUT} is ‚good'
… understand what this means! …

Output *Voltage* of the Differential Amplifier

- If *no current* flows out of the circuit and the output voltage is left free, we have *voltage* gain (the current pulls V_{out} hi/low)

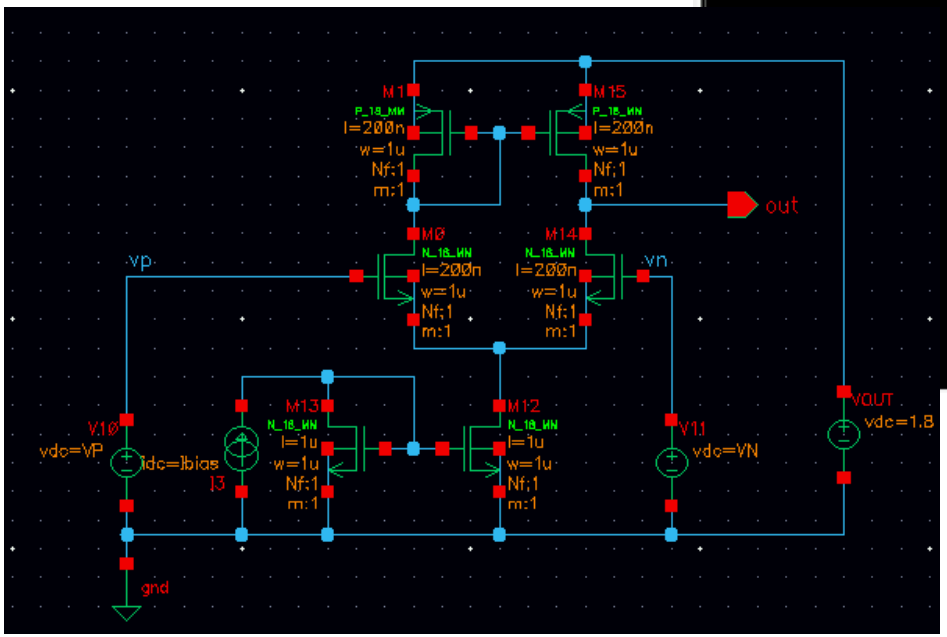


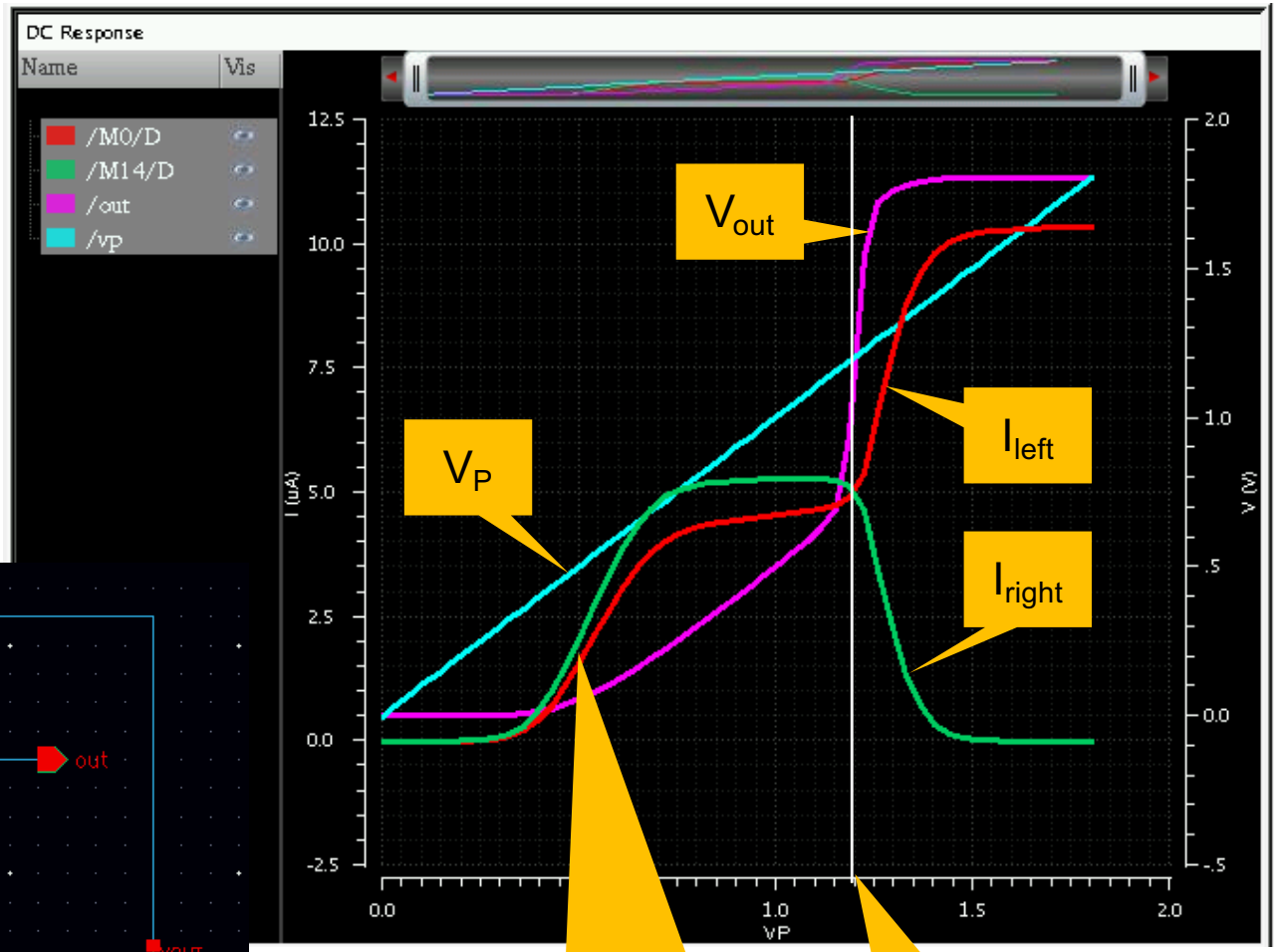


Output cannot go lower than $V_S \sim V_+ - V_T$

Simulation

- VDD = 1.8V
- V_N = 1.2V





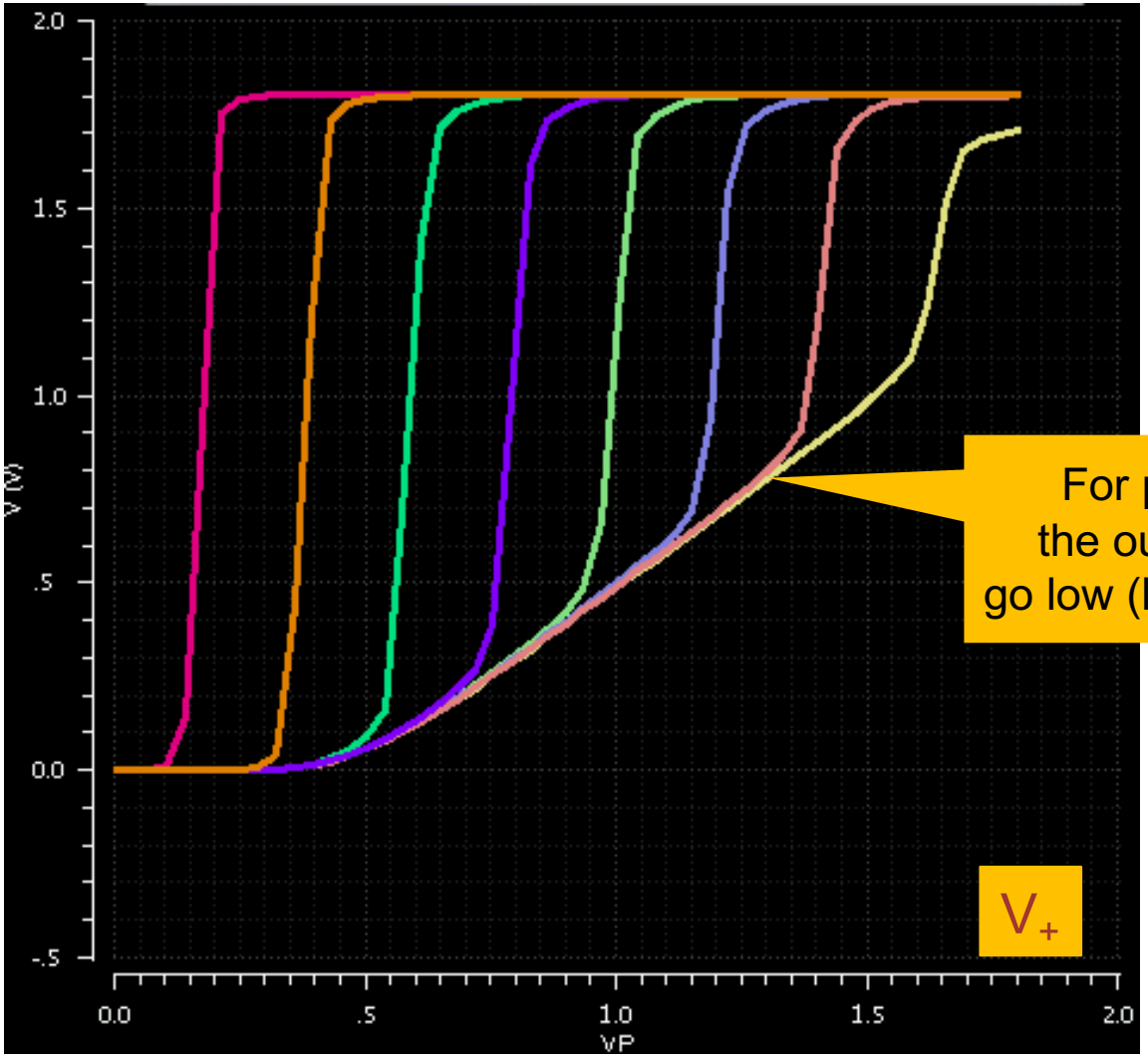
Strange operation here: I_{right} cannot flow because output is low

V_N=1.2V

Sweeping V-

- V- = 0.2, 0.4,...1.6 V

V_{out}



For positive V-,
the output cannot
go low (lower than V_S)

V_+

Gain

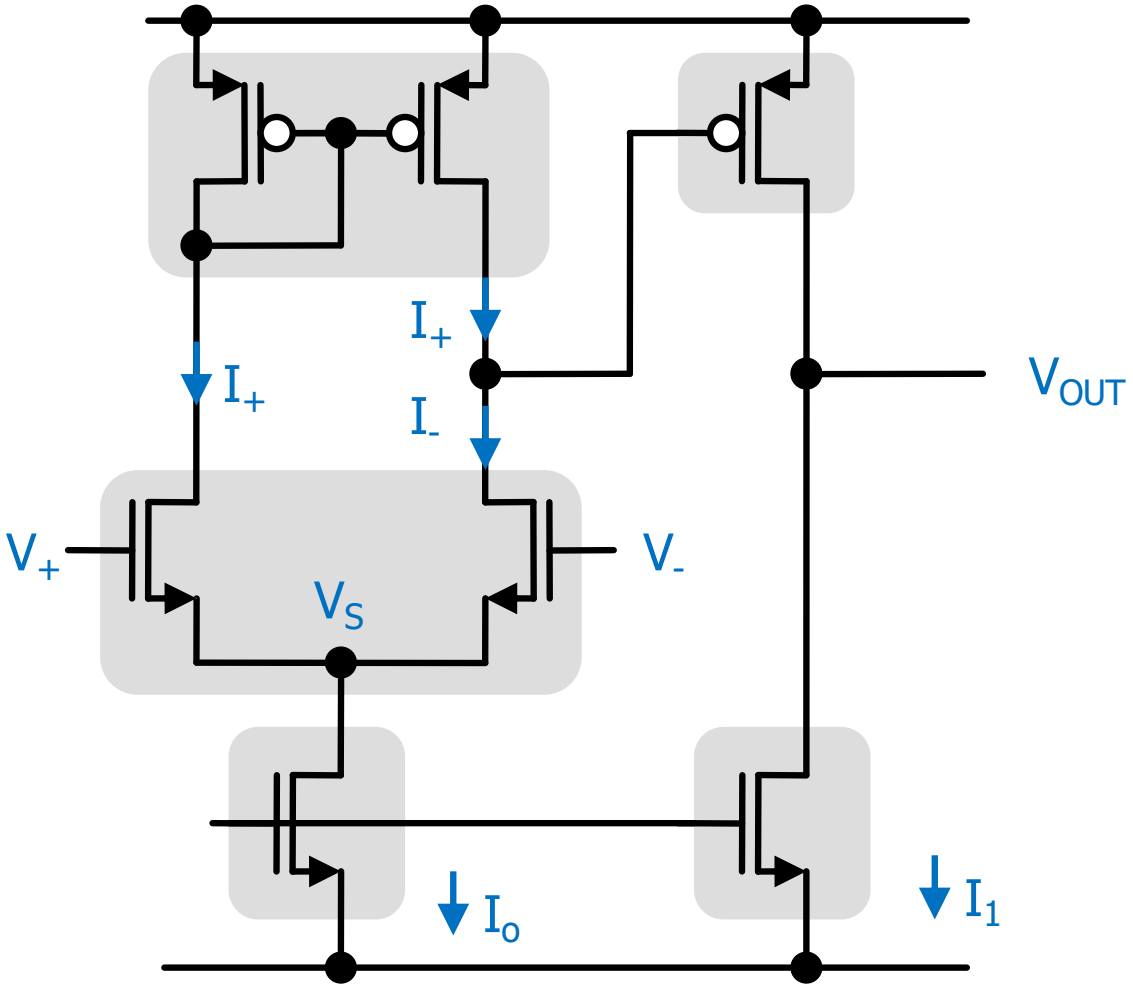
- What is the (voltage) gain?
- To first order, it is – as before – the g_m of the *input* transistor(s) multiplied with the total impedance at the *output* (i.e. r_{ds} of the current mirror output in parallel to r_{ds} of the diff. pair)
- (The output resistance on the left branch do not matter, because the voltage there is kept nearly constant by the diode connected PMOS upper left…)

Comments

- Understanding the large signal behaviour for very different V_p,V_n is important, but in practical circuits, feedback is often applied so that $V_p = V_n$.
- Another important property is the *common mode input range*. This is limited by the V_{GS} of the input pair and the compliance of the tail current source: An *NMOS* differential pair *does not work* any more at *low* (common mode) input voltage.
- Another property is *common mode gain*, i.e. the change in output voltage if both inputs are changes simultaneously. In an ideal amplifier, common mode gain is 0.
- If the amplifier is loaded with a resistive load, gain drops. (as for the gain stage).
  - Therefore a source follower is sometimes added.
  - Stability in feedback circuits is then more tricky. Compensation methods are needed.

More Gain: Diff-Amp with Gain Stage

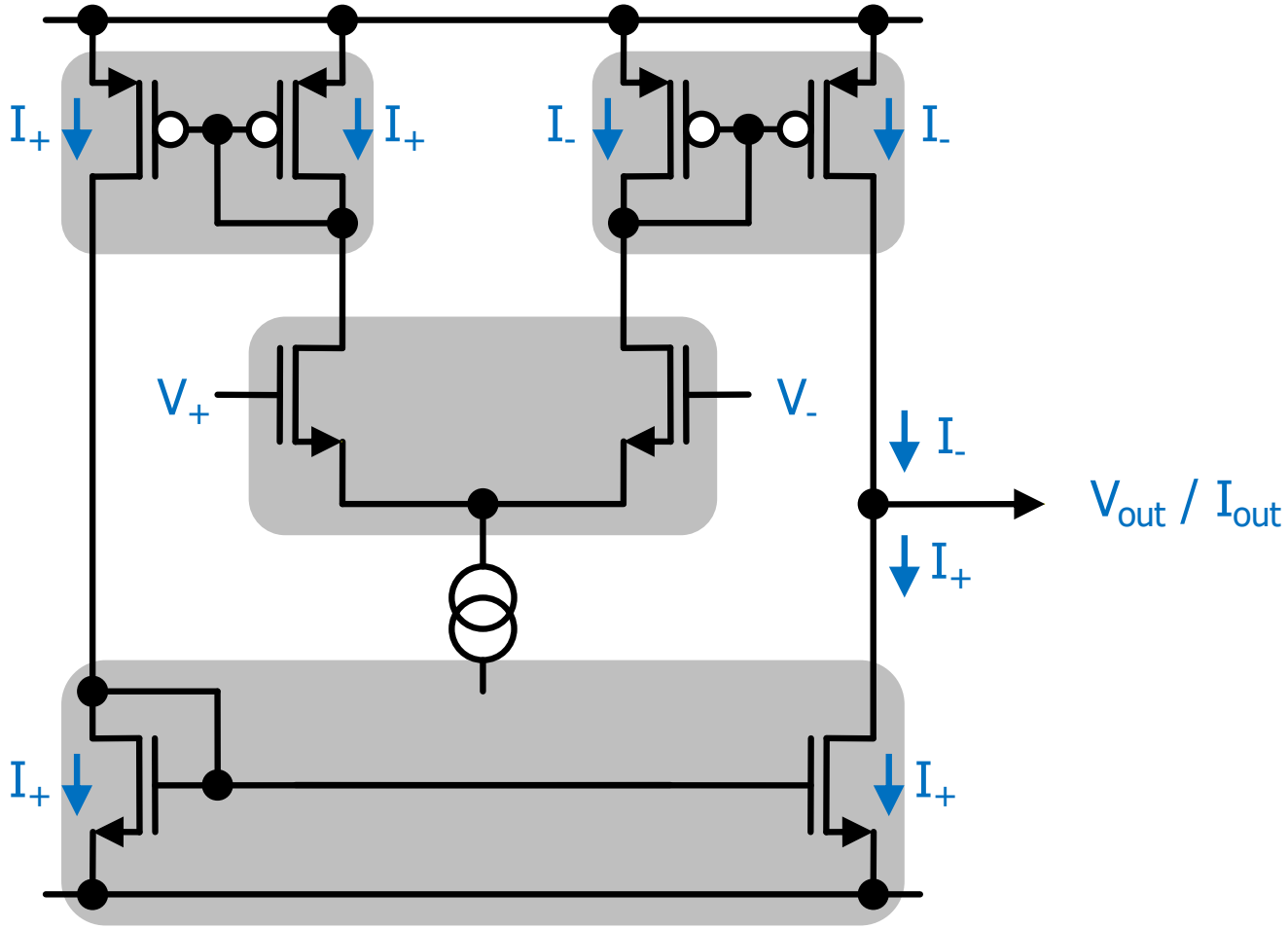
- The differential amplifier is often followed by a gain stage
  - This two-stage design has two ‚main' poles and may need compensation if used in feedback configuration



- The 'steep' part of the transfer function of the first (differential) stage should coincide with the 'steep' part of the second stage!
- This can be achieved (for 3x equal PMOS) with $I_0 = 2 \times I_1$, so that $I_+ = I_- = I_1$ at the switching point.

Differential Pair + Current Mirror

- The problem of limited output voltage swing for high input common mode can be solved by mirroring the currents:



Alternative topologies

- Many topologies are possible, using mirrors and cascodes
- For instance this ‘folded cascode’ configuration