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# Layout Introduction

# Technology, Basic Rules, MOS

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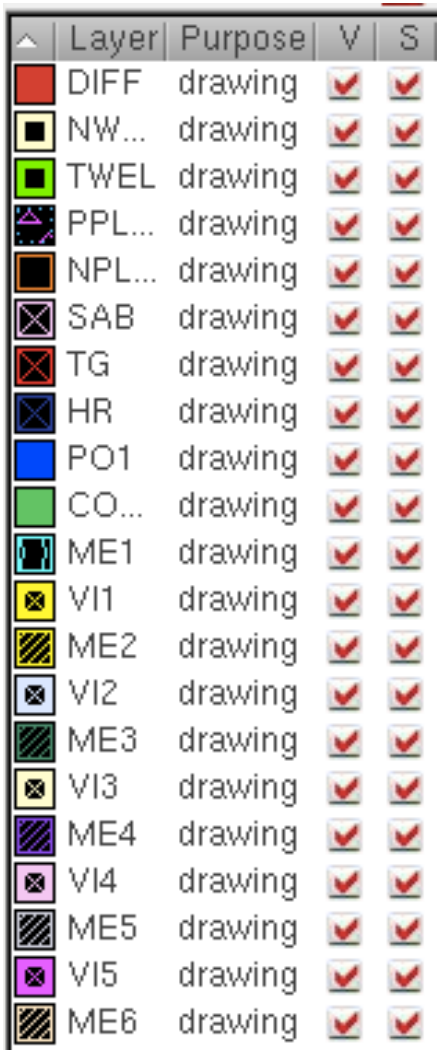
# Layers in Cadence

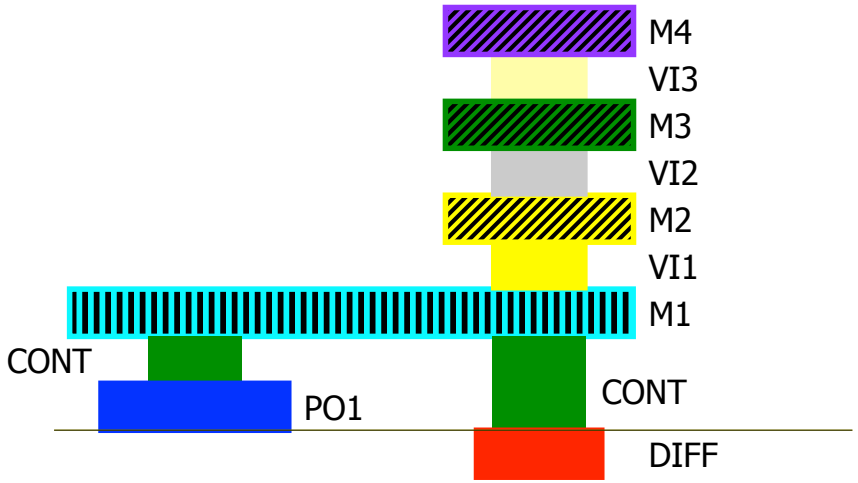
- *Layers* (as shown in the LSW) can have several purposes:
  - Define real shapes (metal)
  - Define cut-outs (slots)
  - Define implantation regions (well, drain,..)
  - Change the meaning of another layer (e.g. change the thickness of a gate)
  - Define additional layout information
    - size of the cell ('instance')
    - areas where a LOGO can be placed
    - Fix where the terminal of a resistor is
    - …
- Often, the combination of several layers defines what happens:
  - metal on chip = *ME1.drawing* – *ME1_CAD.slot*
  - P-Implant = *DIFF.drawing* + *pplus.drawing*
  - …



# The Simplest Layers: Routing Layers

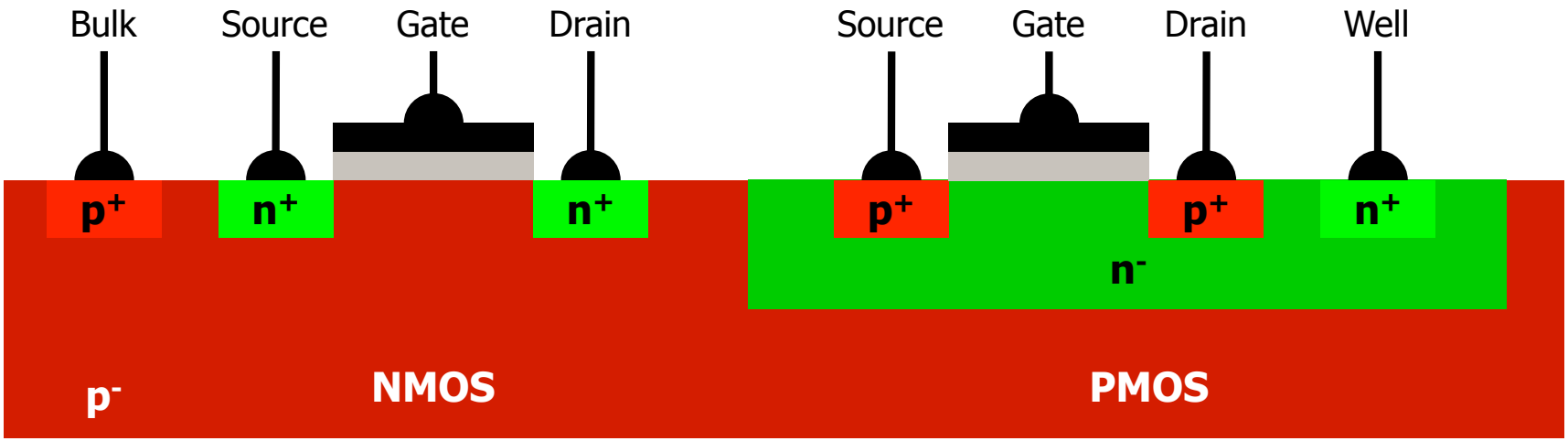
- The technology we are using has 7 routing layers:
  - 1 poly silicon layer at the lowest level (*PO1*)
  - 6 metal layers (*ME1..ME6*), *ME6* is topmost
- The metal routing layers are connected with *vias*
  - *VI1…VI5*: *VI1* connects *M1* to *M2* etc.
- Poly routing **OR** substrate is connects to *M1* with *CONT*

| Layer | Purpose | V | S |
|---|---|---|---|
| PO1 | drawing | ✓ | ✓ |
| CONT | drawing | ✓ | ✓ |
| ME1 | drawing | ✓ | ✓ |
| VI1 | drawing | ✓ | ✓ |
| ME2 | drawing | ✓ | ✓ |
| VI2 | drawing | ✓ | ✓ |
| ME3 | drawing | ✓ | ✓ |
| VI3 | drawing | ✓ | ✓ |
| ME4 | drawing | ✓ | ✓ |
| VI4 | drawing | ✓ | ✓ |
| ME5 | drawing | ✓ | ✓ |
| VI5 | drawing | ✓ | ✓ |
| ME6 | drawing | ✓ | ✓ |



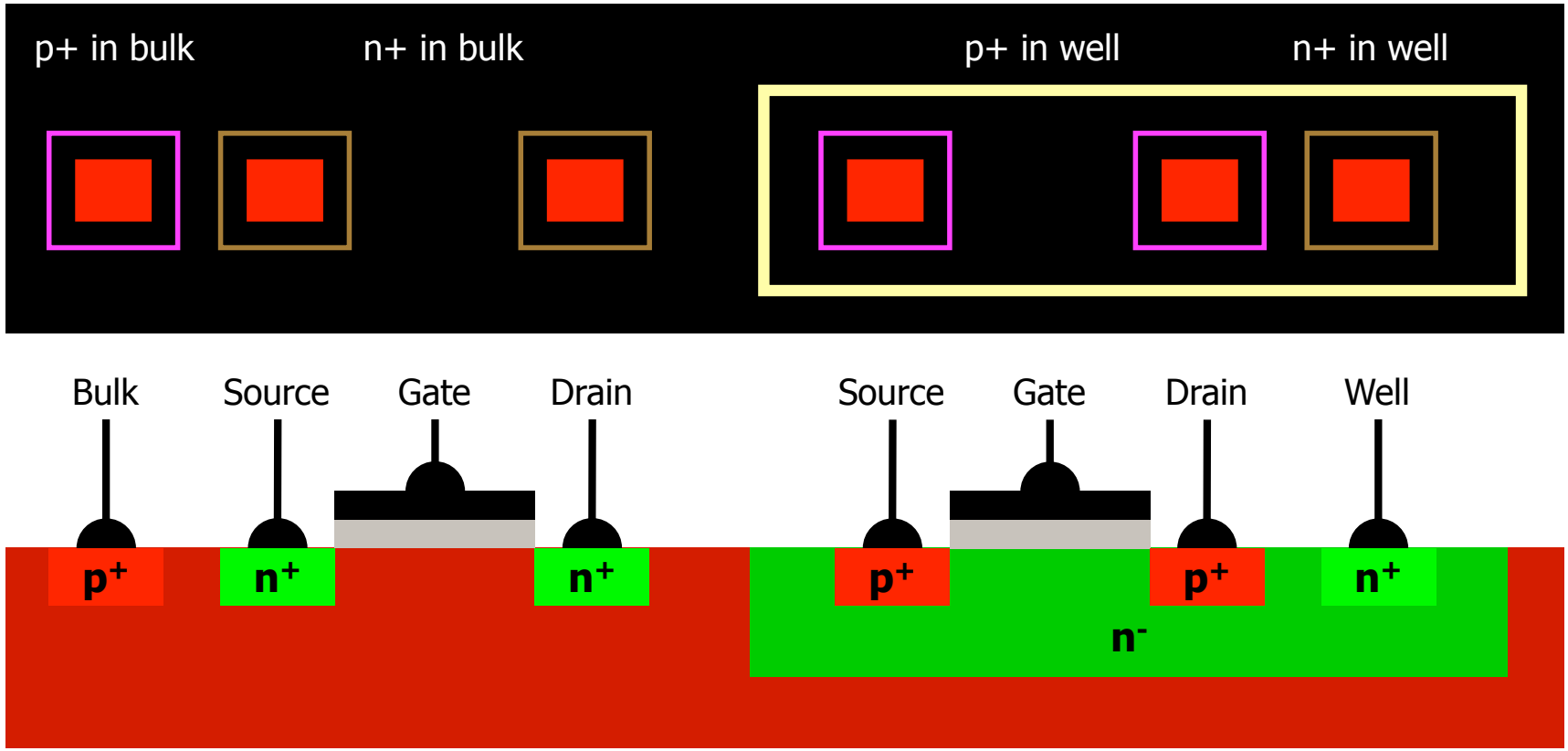
# Reminder: NMOS / PMOS (p-bulk Technology)

- PMOS sits in a (low doped) n-Well
- The NWELL o a PMOS is connected with a N+ 'Well' contact
- The substrate of a NMOS is a P+ contact in the 'bulk'
  - This is the same for all NMOS
- (The technology also provides a NMOS with a separate WELL, see later)



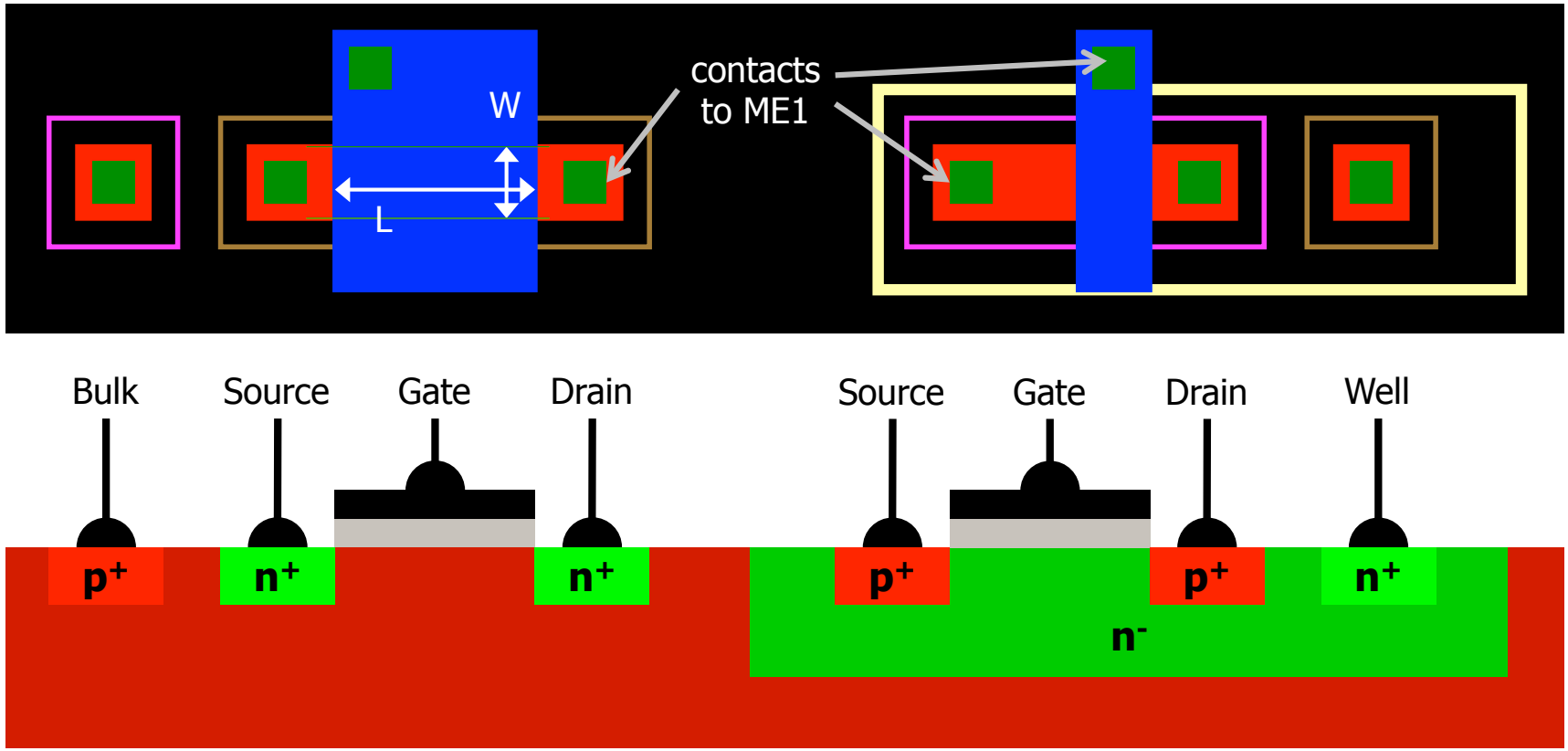
# Implantations

- *NWELL* is a separate layer
- All 'strong' implantations (no wells) are defined by *DIFF*
- The implantation TYPE is defined by *additional* layers *pplus* or *nplus* *enclosing DIFF*:



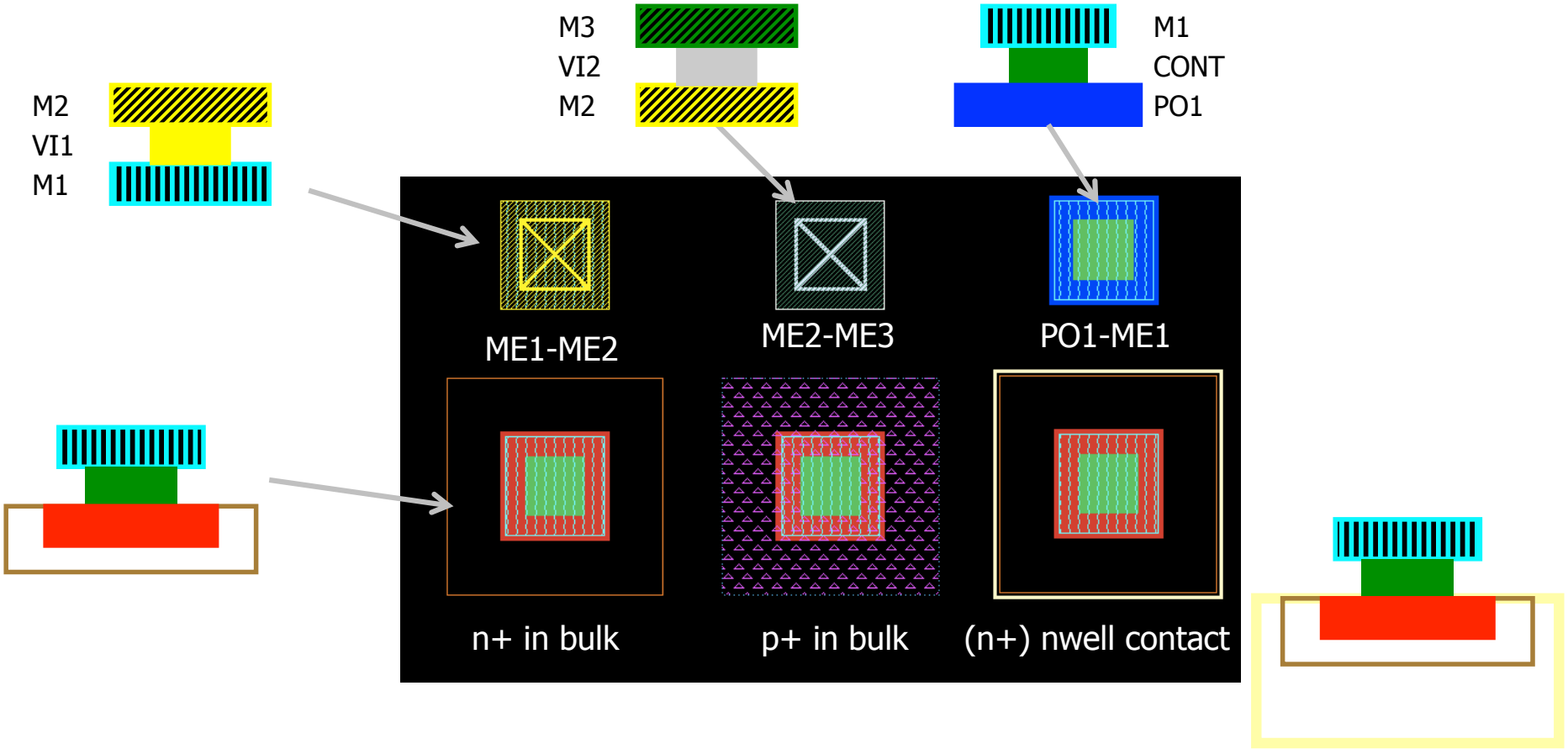
# MOS Gate

- The gate is produced in 'self aligned' technology (see later) and is actually drawn on top of *diff*:



# Vias and Contact Cells

- Because vias, contacts and p+, n+, nwell contacts are often needed, they are available as prepared cells
  - Press 'o' in the layout editor



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# DESIGN RULES

# Design Rule Check

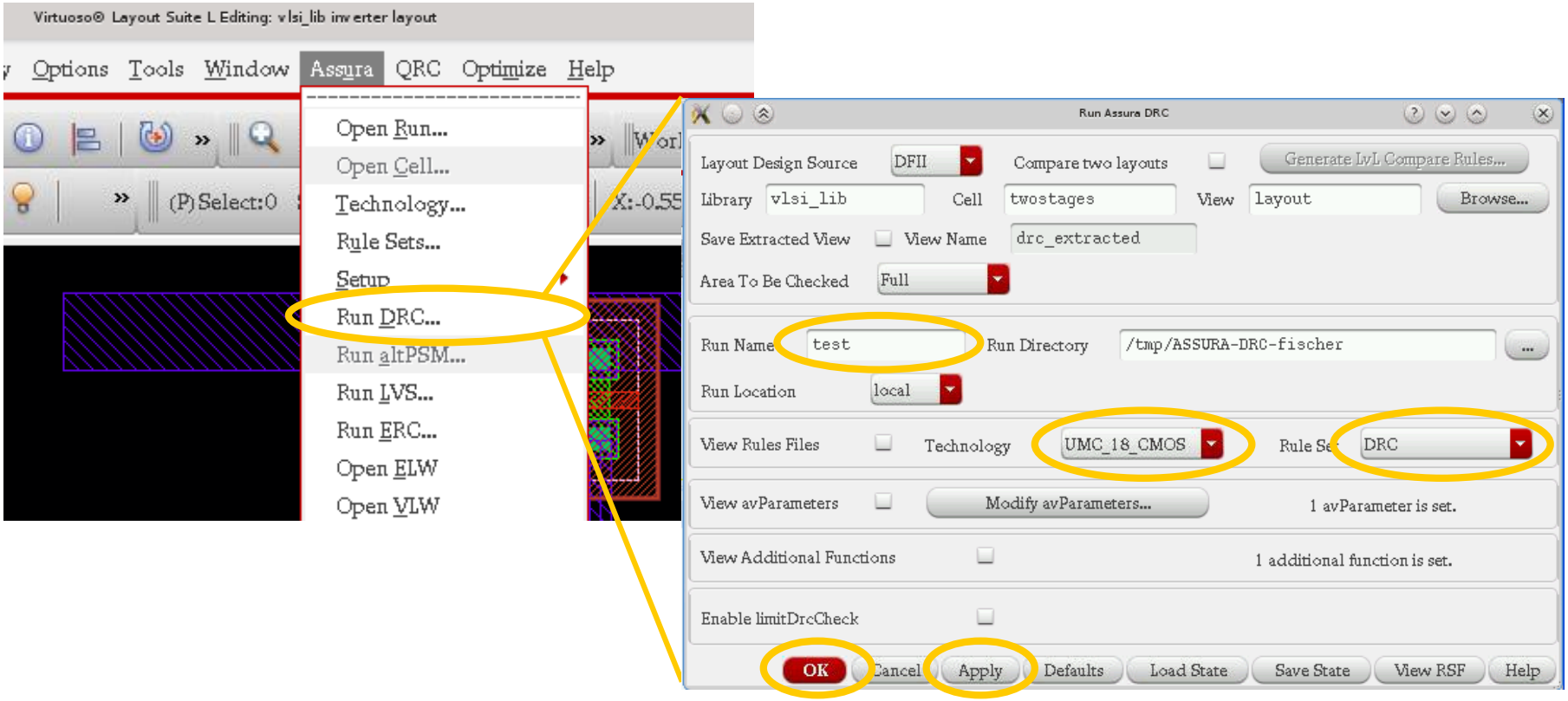
- You can draw any shape, but often you will violate rules set up by the vendor
- You can check your layout with a tool called

Design Rule Check (DRC)

- It checks your design based on a set of rules provided by the vendor (written down in a file using a special syntax)

# Starting the DRC

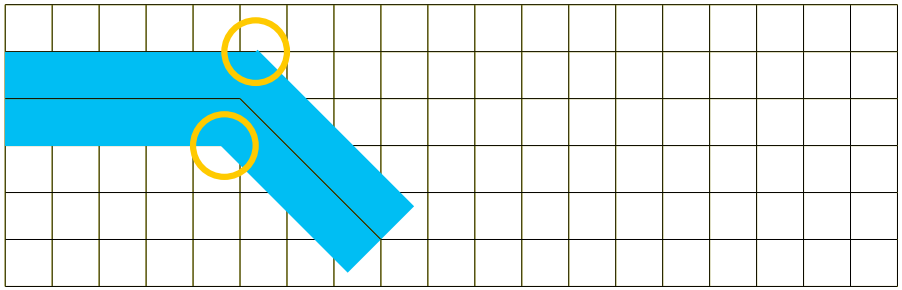
- Select from the top menu Assura → Run DRC…
  - Make sure *Rule Set DRC* is selected
  - Make sure you have set a *run name* (otherwise you get a strange error)
  - *OK* closes the window, *APPLY* keeps it



# General Rules

- **Angles**:
  - Usually only *multiples of 45 degree* are allowed

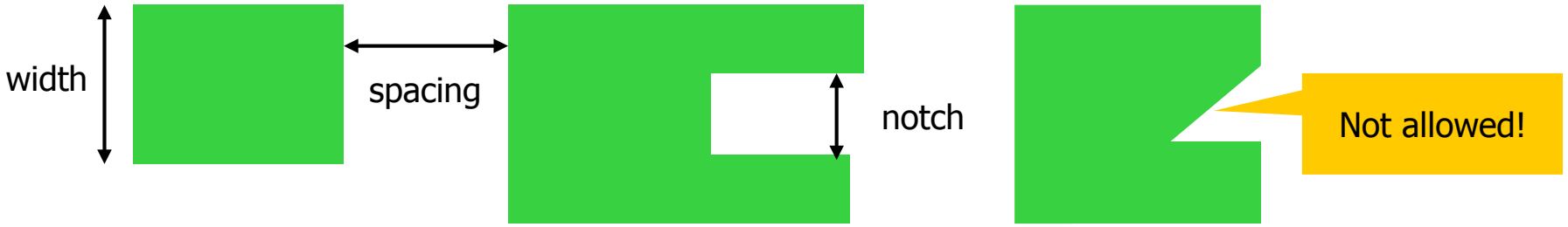
- **Grid**:
  - All corner points must lie on a minimal *grid* (at least when the chip will be produced). For us: 0.01 (µm)
  - Otherwise an 'off grid error' is produced
  - Attention: If a *path* of width *d* is drawn in 45°, the corners can be off grid (on $\sqrt{2}$ x b/2) (depending on 'flatten' algorithm). Better draw polygons!



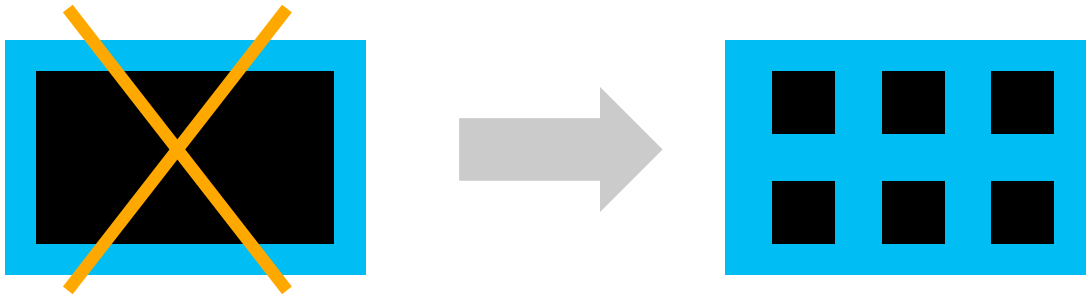
  - Circles can be drawn, but are converted later to Polygons with on-grid points, causing trouble

# Rules in One Layer

- Caused by manufacturing limits (lithography, etching,..)
- Rules: *Spacing, Width, Notch* (='Kerbe') between *same* net
  - Finest structure is Poly-silicon for gates

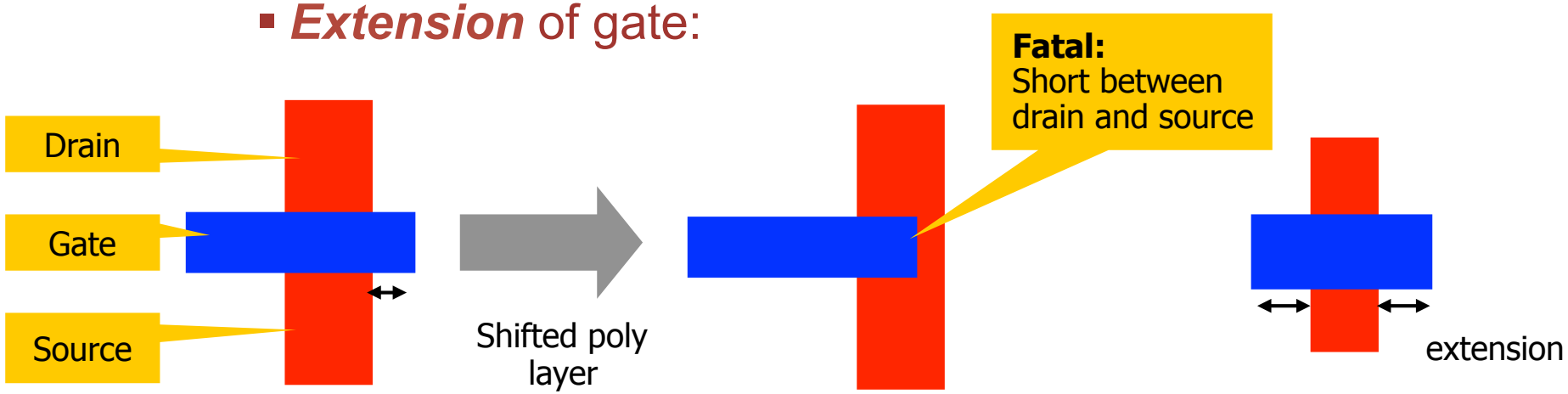



- Some structures have '=' rules, i.e. must have *exactly* a fixed size. Prominent example: contacts and vias
- Larger vias must therefore be created by repetition ('mosaic'):

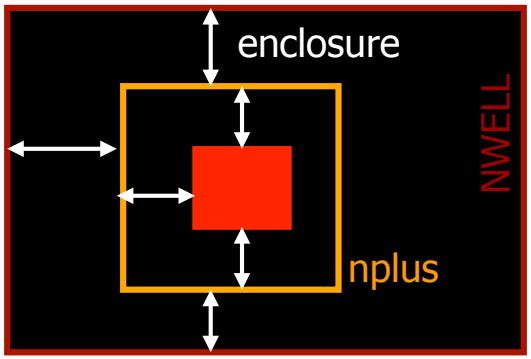


# Rules Between Layers

- Caused by alignment precision of different masks
- ***Extension*** of gate:




- **Enclosure / Overlap**
  - *NWELL* enclosure of *nplus* and *nplus* enclusore of *DIFF*




‘*Metal* enclosure of *via*: