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HEIDELBERG

Exercise:
DRC

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SOME REMINDERS

Reminders

- When *gravity mode* is on, the cursor snaps to various shapes.
  - Toggle gravity mode with ‘g’ (Options → Editor...)
  - Better turn it off...
- Toggle between *full* and *partial selection* mode with F4
- Snap mode:
  - Normal is ‘*orthogonal*’: edges can be only in x- or y directions
  - To change, invoke the options menu with F3 when drawing or moving
- Snap grid
  - Change snap grid spacing in editor options (‘e’)
  - Use as coarse grid as possible. Min = 0.01 µm (in this techno.)

Reminder: Shapes / Contacts / Vias

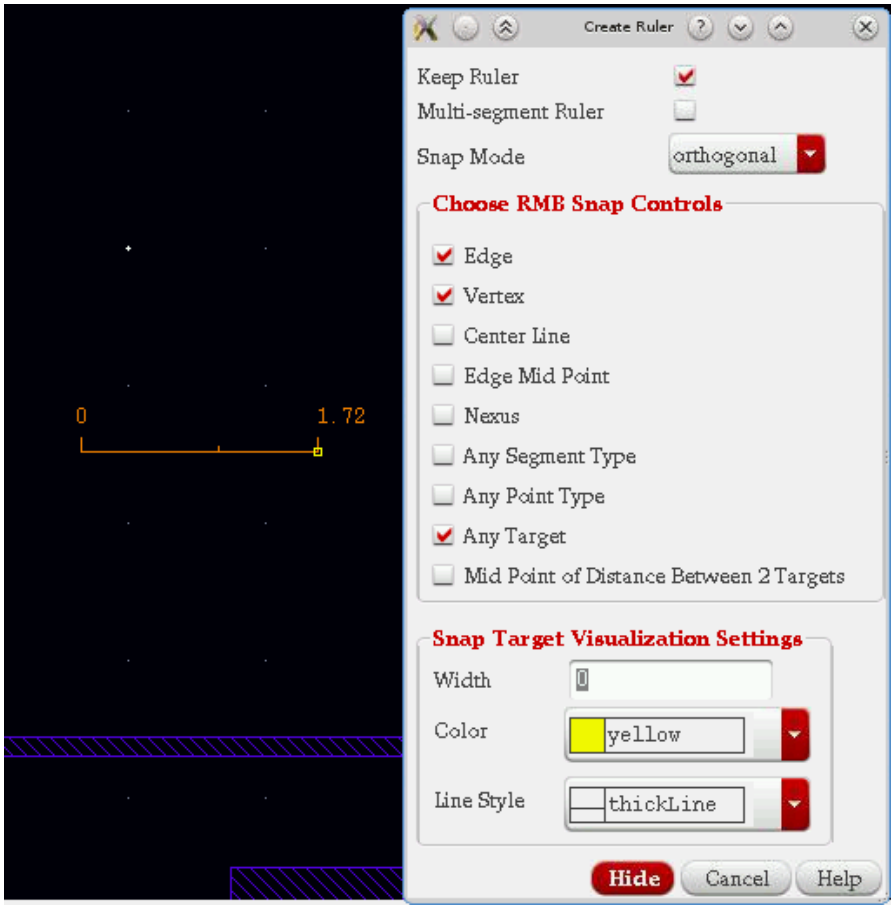
- Shapes are
  - Paths (‘p’)
  - Rectangles (‘r’)
  - Polygons (‘Shift-P’)

- To create a contact or via, use Create → Vias (‘o’)
  - Select the layer pair you need
    - it contains shapes on 3 layers automatically

  - You can also create larger arrays
  - In ‘stack’ mode, you can connect across several layers (for instance M1 → M4)

Measuring Distances with the Ruler

- The ruler can be displayed with Tools → Create Ruler (‘k’)
- Invoke the option menu with F3 (sometimes twice)
  - Better switch off all snap options
- Rulers are kept with the ‘Keep Ruler’ option
- Clear all rulers with ‘Shift-K’



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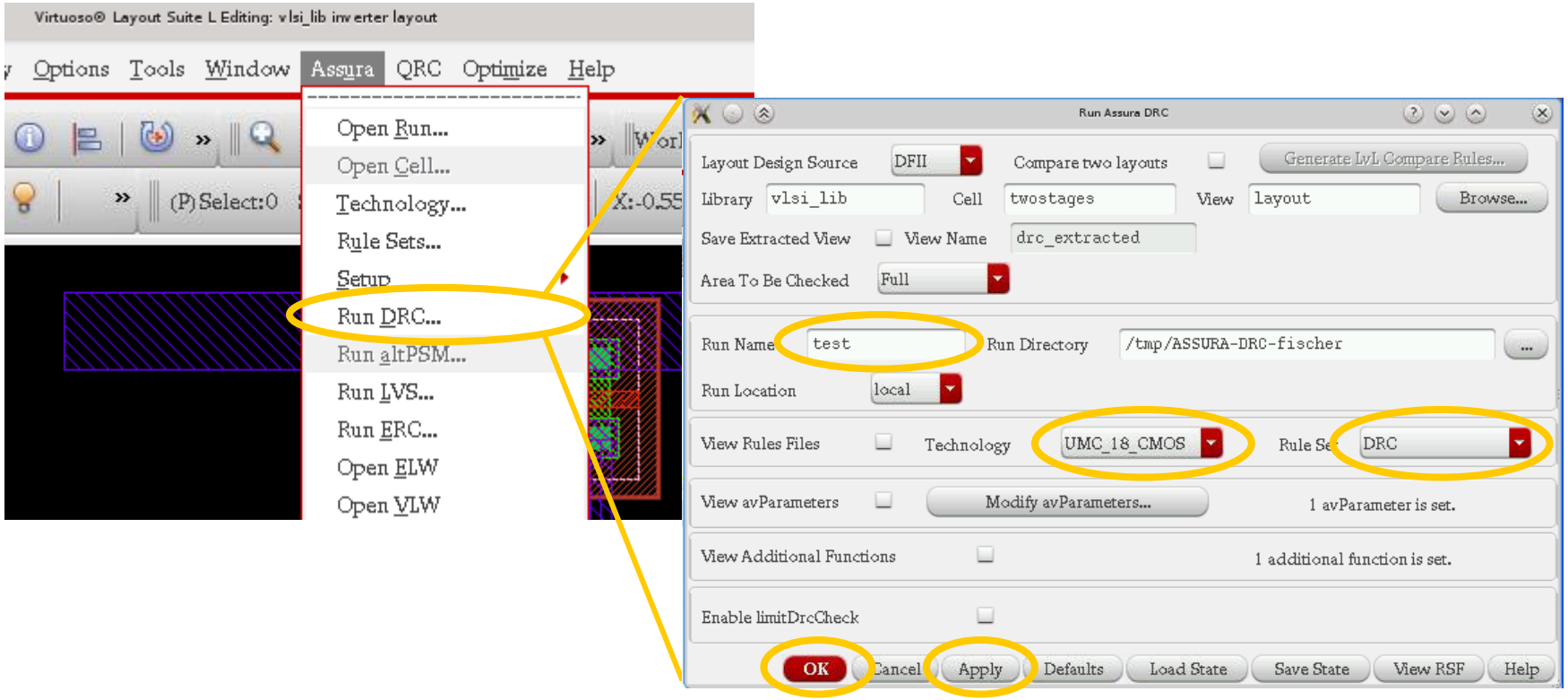
DRC

DRC Design Rule Check

- The Design Rule Check verifies that the geometric rules are respected.
- The rules are specified in a text file

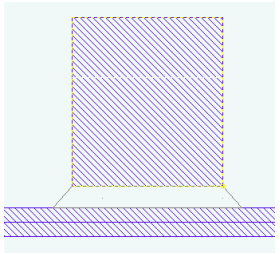
Starting the DRC

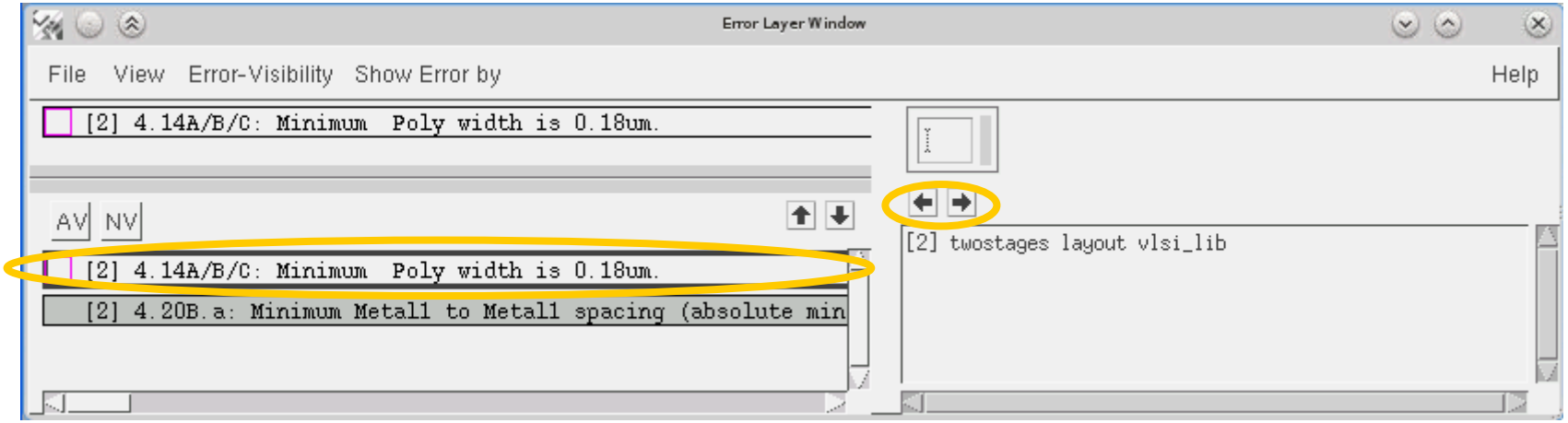
- Select from the top menu Assura → Run DRC
  - Make sure *Rule Set DRC* is selected
  - Make sure you have set a run name
  - *OK* closes the window, *APPLY* keeps it



Viewing DRC results

- The Error Layer Window (ELW)
  - Select an errors type (left)
  - The arrow on the right skip from error to error.
    They are highlighted and zoomed in the layout editor

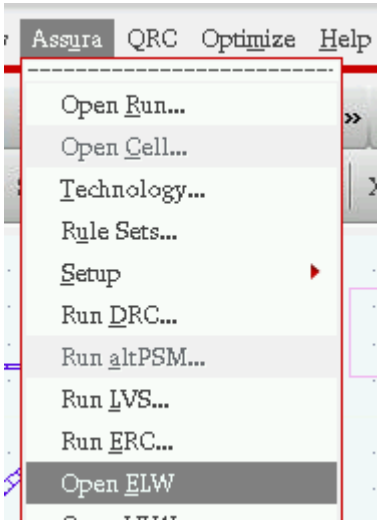




- The ELW cannot be closed with the  button (bug!)
  - Use File → Close ELW

Re-loading a DRC

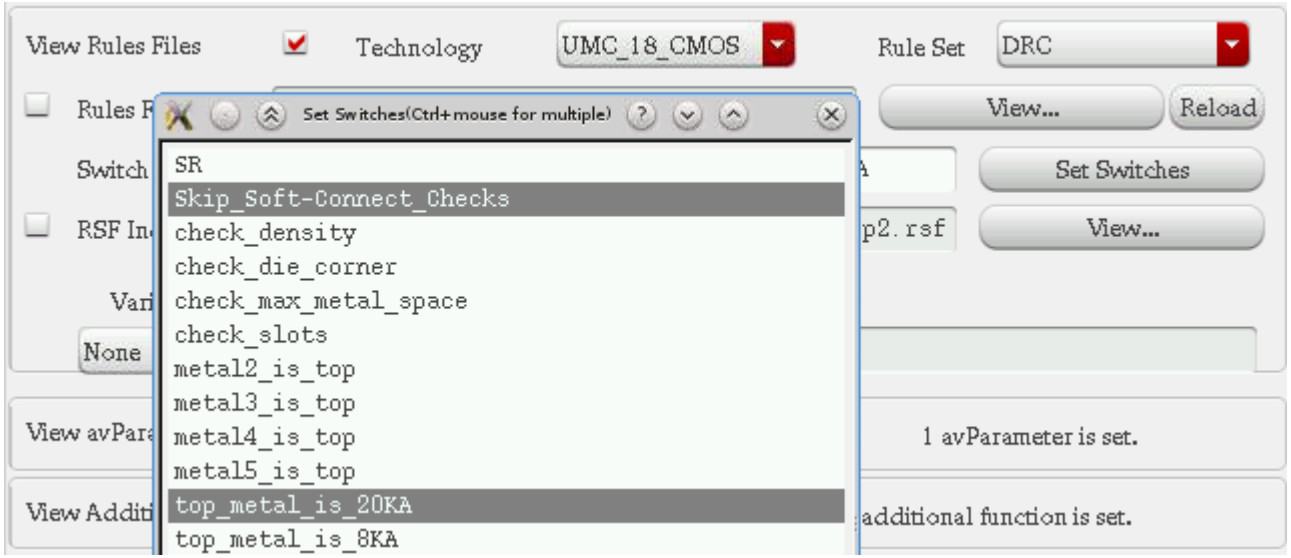
- If the ELW has been closed, it can be re-opened with
  - Assura → Open ELW



- The run can be closed explicitly in the same menu
- An old run can also be opened there.

Advanced: DRC Options

- You can set specific DRC options
  - Check the ‘View Rules File’ box
  - Select ‘Set Switches’
  - Chose from the options



  - We use mostly a thick top metal technology (‘20kAngström’)
  - The check_xxx options are only used at the end of the design process...

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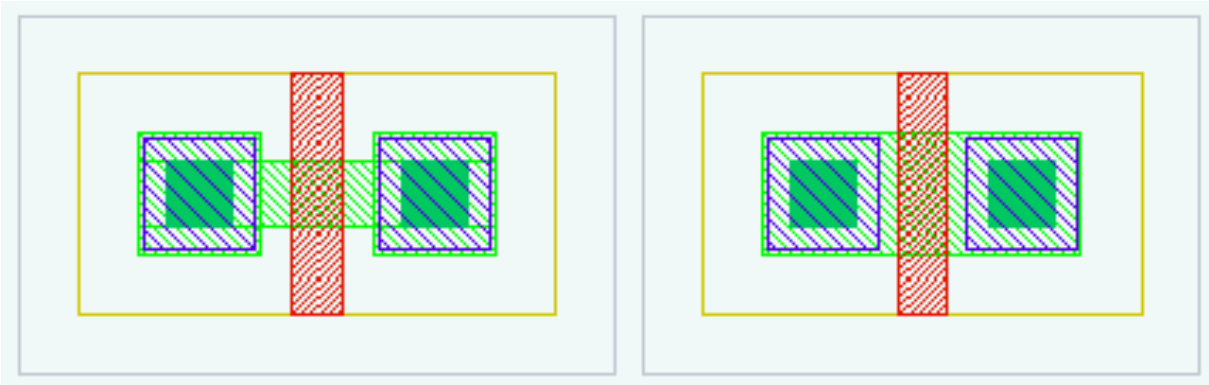
EXERCISES

Exercise A: Minimum Rules

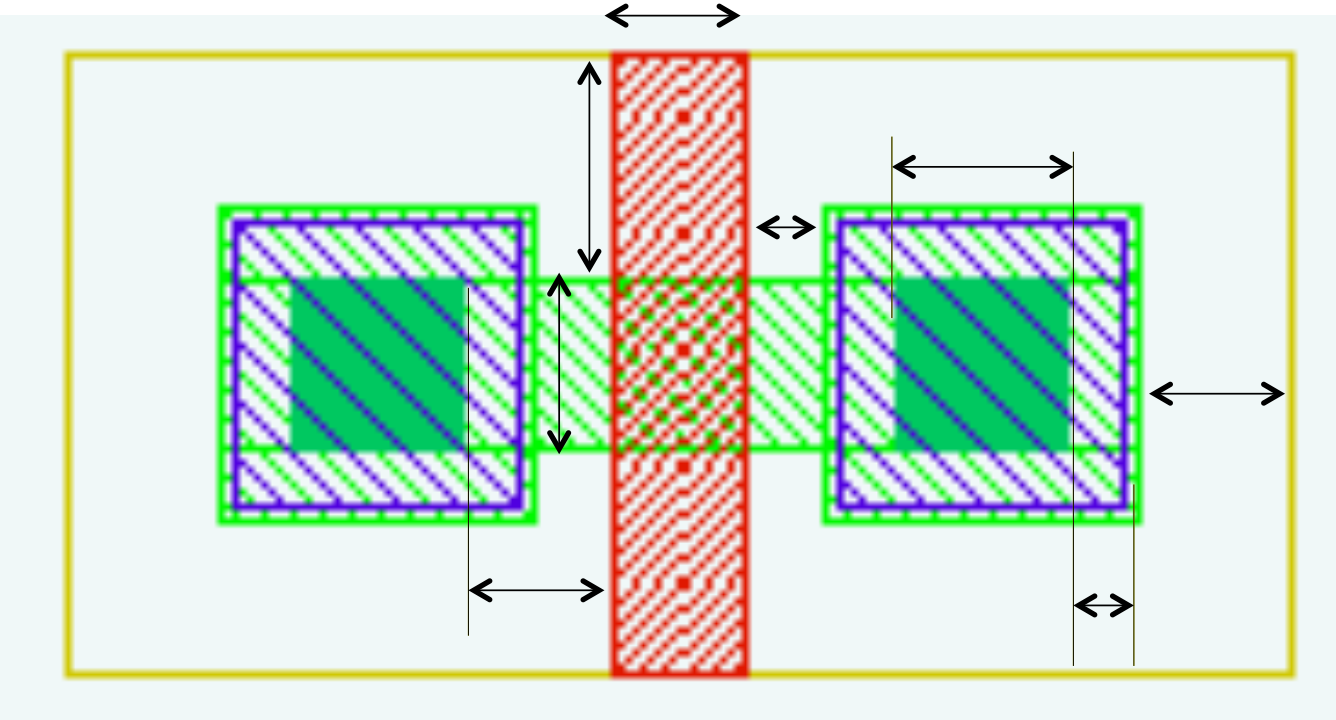
- Get a N_18_MM NMOS with minimal size (240nm/180nm) from the library
- Flatten the instance (Chose Edit → Hierarchy → Flatten, make sure you allow flattening of PCELLs)
- Try to make the layout smaller at various places and observe the DRC errors you will get.



- Increase the width of the MOS to 0.44µm and try to make it 'shorter'

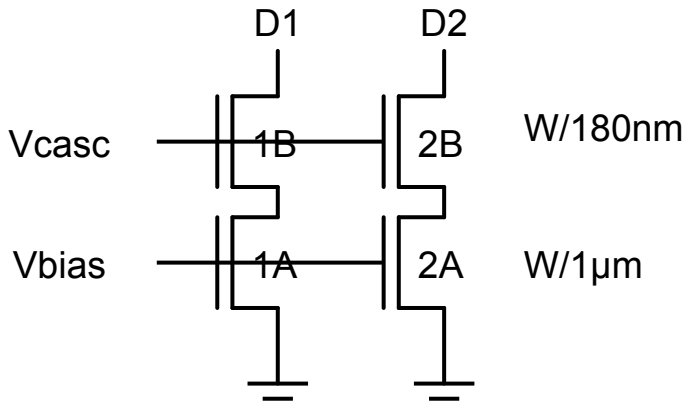
Exercise A: Minimum Rules

- Some important design rules are shown here
- Determine the value from the DRC violations you get



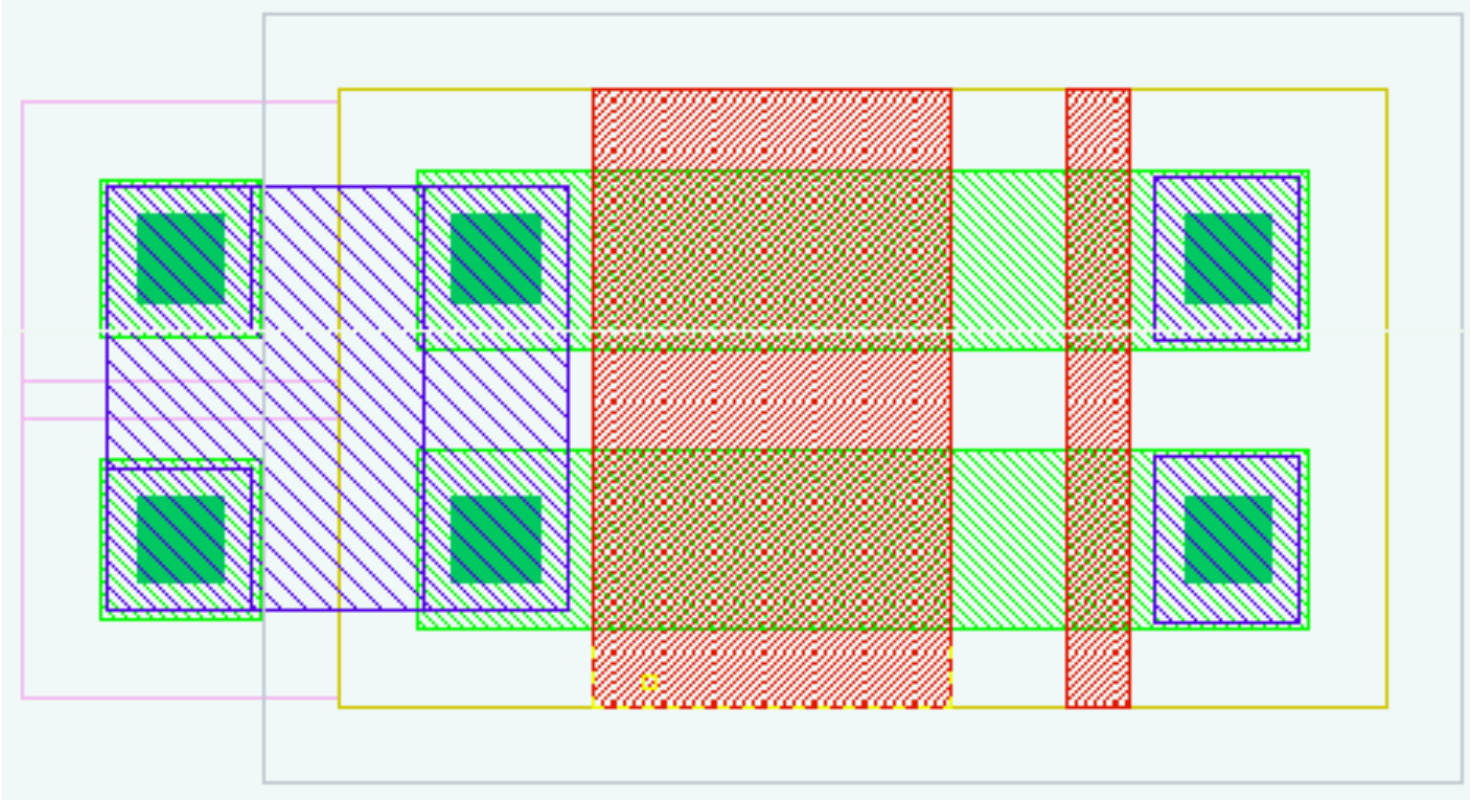
Exercise B: Cascoded MOS

- Make the layout of the parallel connection of two cascoded NMOS transistors:



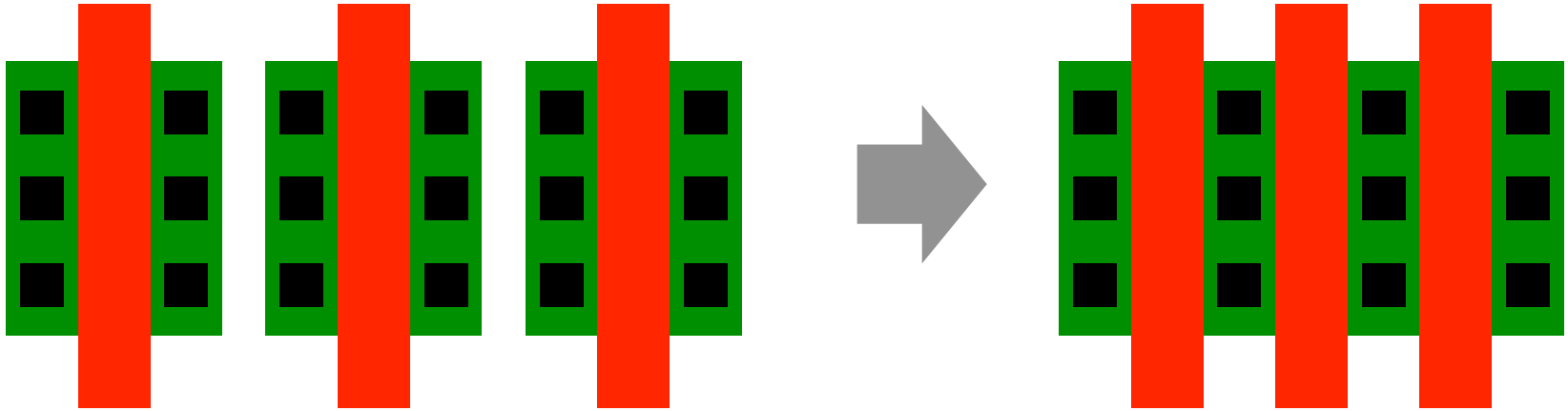
- Note the given lengths! Use W=500nm to start with
- You can start with a library MOS, flatten it, and change it.
  - Make sure you have SYMBOL/MM layer turned on
- Eliminate the contacts between the series devices A and B
- What is the minimal distance between left and right devices?
- What is the minimal W such that exactly 3 contacts fit into the source?

Exercise B: Solution



Exercise C: Wide ('folded') NMOS

- For a clock-buffer, you need an NMOS with W=50µm.
- Drawing it as one device gives a very asymmetric shape.
- The common solution is to use several MOS of smaller W and place them side-by side.
  The layout can be much more compact by overlapping the sources and drains:



- Connect all gates.
- How can you best connect the drains/sources?

Exercise D

- Common Centroid geometry