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Some Comments on Analogue and Mixed Mode Design

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Challenges in Analogue Design: Noise

- **Noise** (physical, unavoidable)
  - Thermal noise in resistors and MOS is rather well described and quite technology independent
  - 1/f noise in MOS is technology dependent, less well modelled
  - More details in lecture 'Advanced Analogue Building Blocks'
- Remedies:
  - Chose insensitive circuit topologies, avoid resistors
  - Reduce noise by reducing g_m of MOS where possible (for instance in current sources)
  - Reduce Bandwidth to accumulate less noise spectrum
  - Reduce 'relative' noise by increasing current in MOS
- Study with
  - Mathematical analysis
  - AC noise simulation (see later)
  - Transient noise simulation (see later)

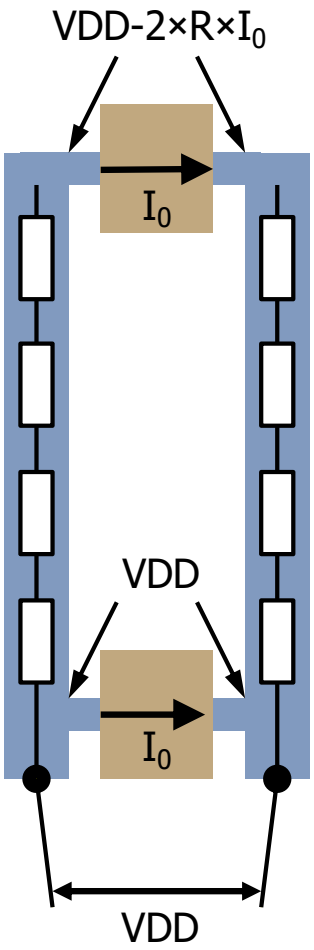
Challenges in Analogue Design: Mismatch

- **Device Mismatch**
  - From fluctuations in fabrication
    → Mismatch in current mirrors
    → Offset voltage of differential amplifiers
    → …

- Remedies:
  - Use large devices to reduce geometric uncertainties
  - Use identical layout, common centroid, guard devices,…
  - For MOS: Use high V_{GS} to reduce effect of V_{Th} mismatch
  - See slides on layout…

- Study with
  - Back-on-the envelope calculations using ‘Pelgrom’ model
  - Monte Carlo Simulations (see later)

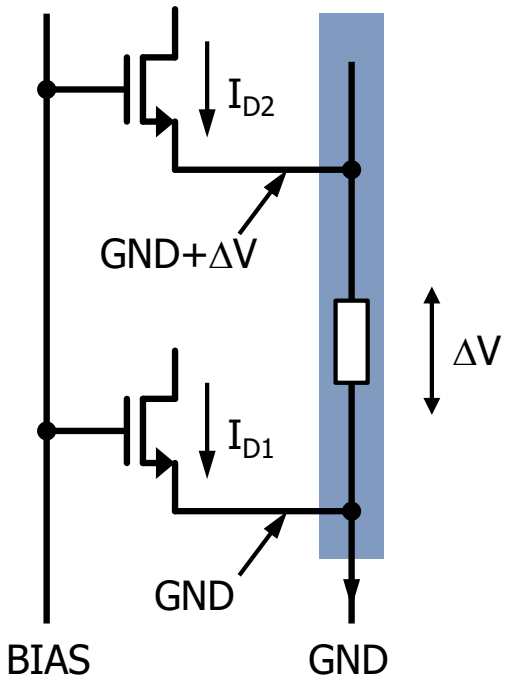
Challenges in Analogue Design



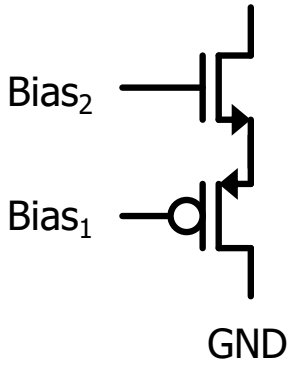
- (Static) power supply voltage drops
  - From 'IR-drop' in supply traces (voltage drop $\Delta U = I \times R$)
- Remedies:
  - Wide / many supply traces (with low resistivity)
  - Multiple bond pads
  - Separate voltage rails for different circuit blocks
  - Voltage drop compensation circuits
  - Circuits with good (low freq.) power supply rejection (PSRR)
  - Multiple (local) references
  - Trimming
- Study by:
  - Simulation of extracted design (or estimated resistances)

Trick: Drop insensitive bias

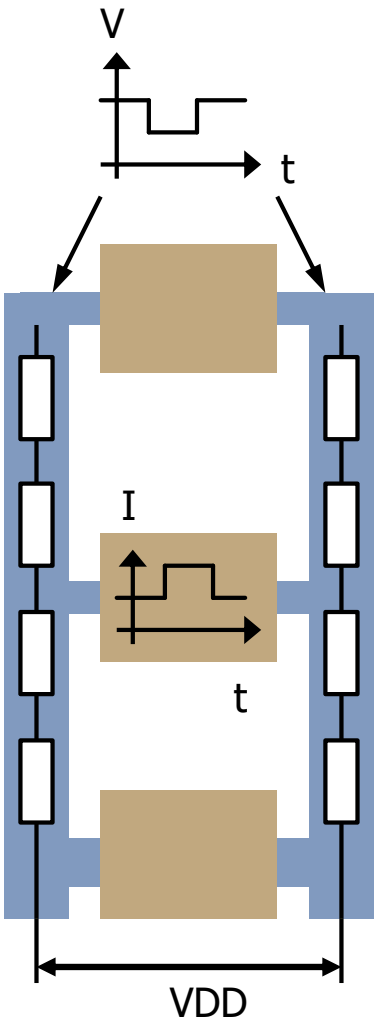
- Problem: When current source MOS are biased with the same gate 'bias' voltage (which has no voltage drop, because no current flows), the different SOURCE voltages (due to voltage drop on GND net) lead to different currents
  - $I_D = f(V_{GS})$.
    $V_{GS2} = V_{GS1} - \Delta V < V_{GS1} \rightarrow I_{D2} < I_{D1}$



- A trick:
  - Use a combination of PMOS and NMOS
  - Current depends (largely) on gate difference
  - Drawbacks: increased mismatch, more voltage needed



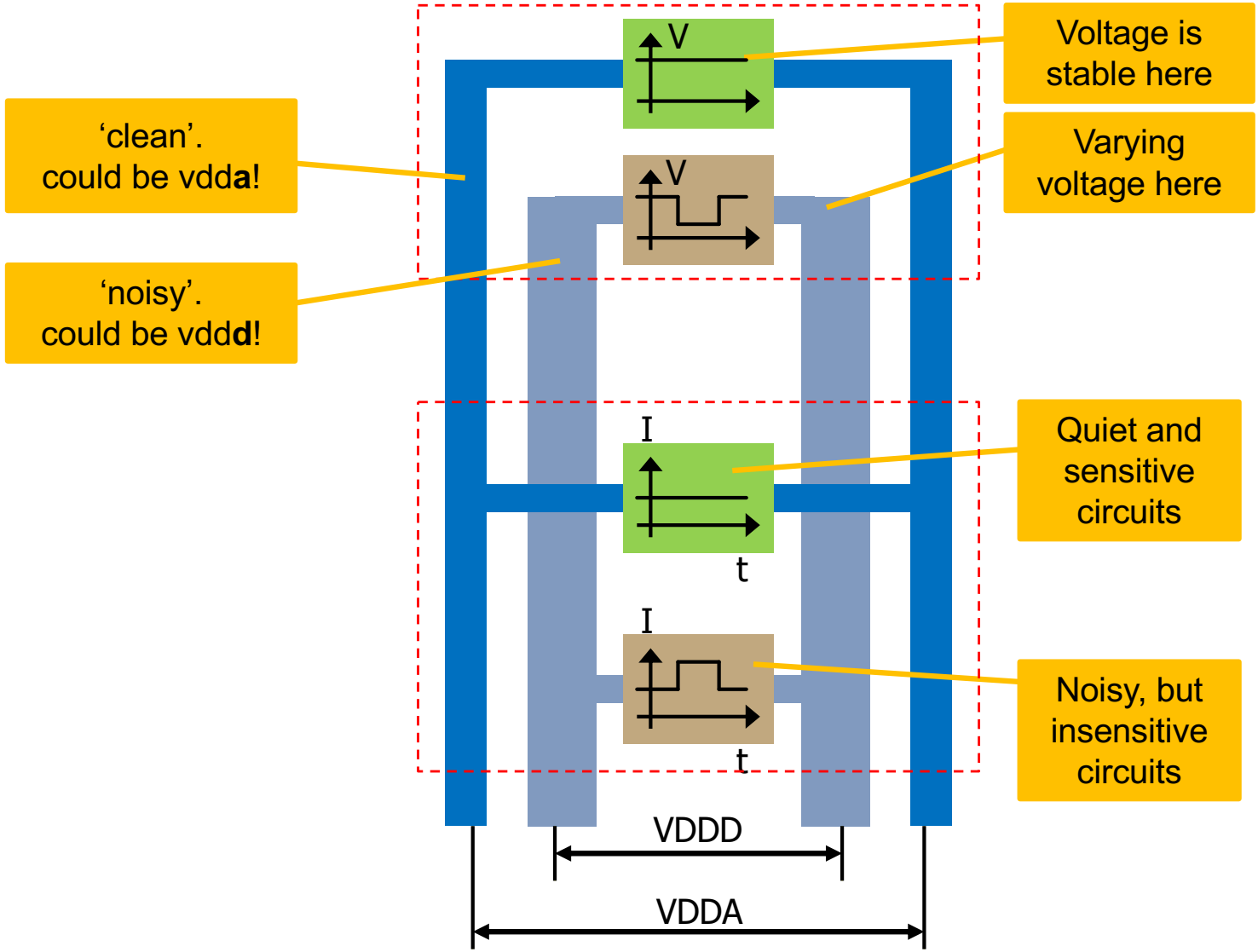
Challenges in Analogue Design



- (Dynamic) power supply glitches
  - Shortly increased current consumption in some circuit parts leads to extra voltage drop and thus quickly changing supply voltage
- Measures against Supply issues
  - Wide traces, multiple bond pads
  - Separate supplies or supply traces
  - Local decoupling of power (‘energy storage’)
  - Local decoupling of bias signals (between gate and SOURCE!)
  - Circuits with good high freq. ‘power supply rejection ratio’
  - Differential circuits
- Study with:
  - Transient sim. of extracted design (or estimate res.!)
  - Often must simulate large circuits and special situations

Analogue and Digital Supply

- Use ‘clean’ (analogue) and ‘noisy’ (digital) supply nets:



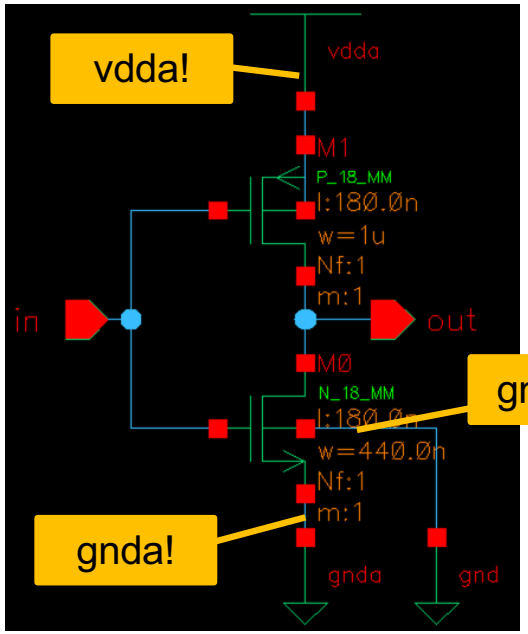
Mixed Mode Challenges

- Digital and Analogue on one chip:
  - Digital activity has very varying currents (clock edges, different data patterns) and leads to dynamic glitches on power supply.
  - Large digital signals can (ac-) couple to sensitive analogue nodes:
    - From trace to trace through parasitic C
    - From MOS gate to channel (cap is high!)
    - From bulk/well to channel

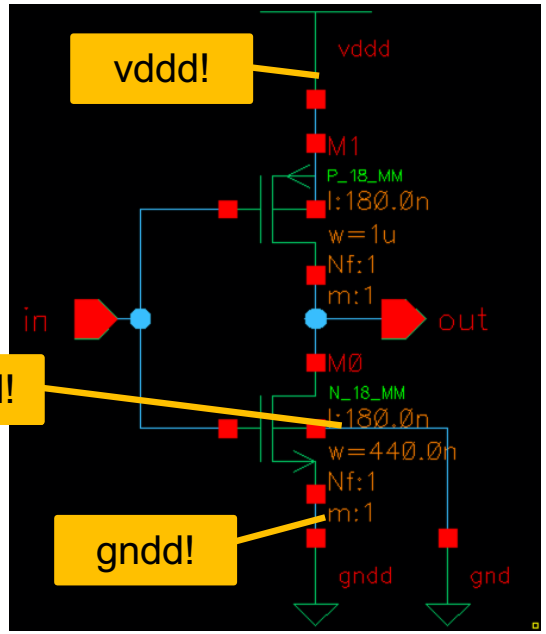
- Some Measures:
  - Separate supply / ground NETs for analogue / digital (vdda, vddd)
  - PMOS well or NMOS substrate (triple well NMOS!) connected to clean (analogue) supply / ground
  - Metal shielding between traces (but connect shield to where ?)
  - Distance between analogue and digital (group analog/digital)
  - Use differential structures so that glitches cancel out
  - …

Using Separate Supplies for Analog and Digital

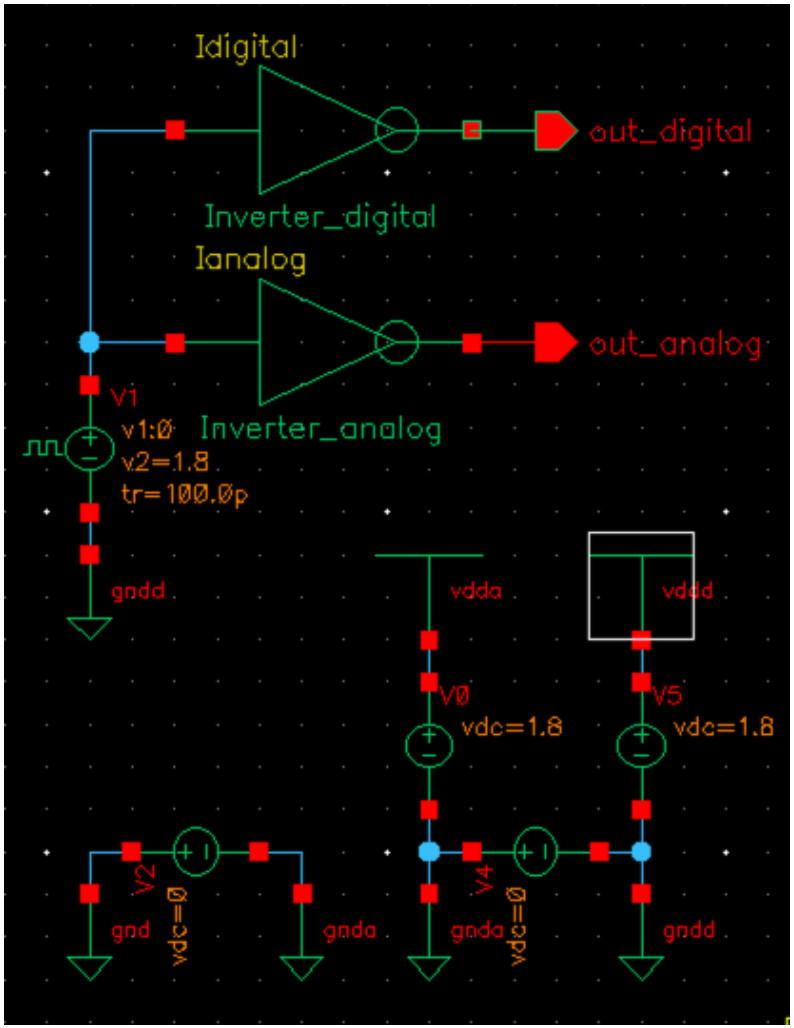
- We assume here the all NMOS are in chip substrate, i.e. have the same bulk potential **gnd!**. (No use of 'triple well')



Analogue Circuit



Digital Circuit



- In simulation, the 3 grounds are at same potential via 0V vdc sources.