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Exercise 2:
Designing with (Schematic) Hierarchy

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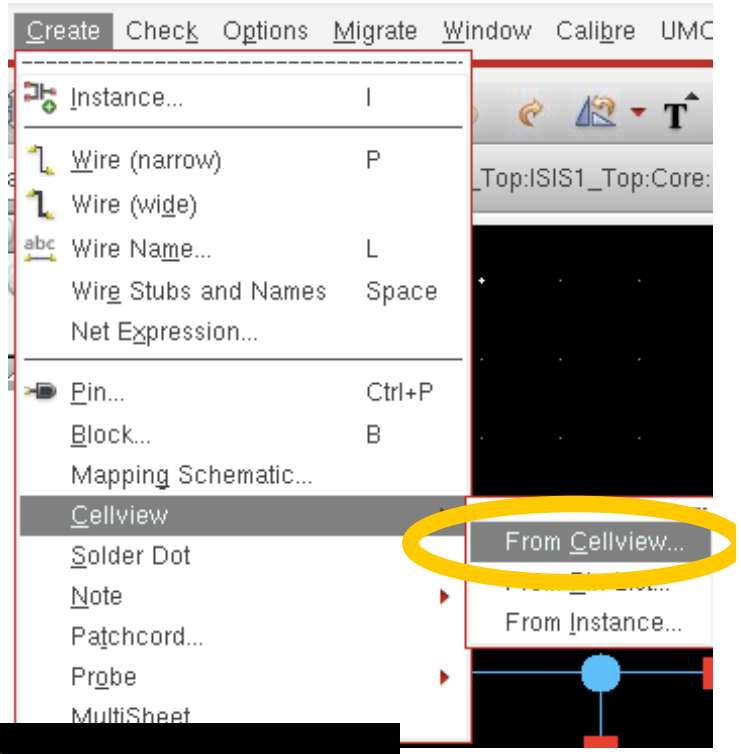
Implementation

1. You can create a *schematic* and a *symbol* view in the same *cell* independently.
   - When you save either cell, the number/names/types of the pins are checked against the other cell.

2. You can also create the 'second' view *automatically*: Create → Cellview → From CellView

- Two further forms are displayed..

- This works in both directions
  - Symbol → Schematic
  - Schematic → Symbol



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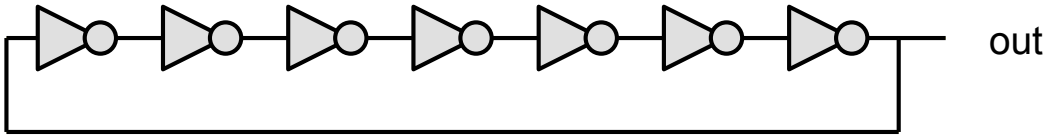
EXERCISE A: RING OSCILLATOR

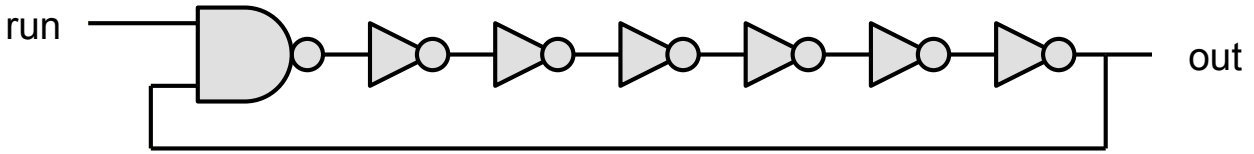
The Circuit

- A Ring Oscillator consists of a chain of N inverters connected to a ring:



- When N is odd (ungerade), the circuit *oscillates*
  - Understand why !
  - What happens if N is even ?

- To start in a well defined state, and to turn on/off the oscillator, we can add a NAND2 gate:



  - You could also add a NOR2 gate. What is the difference ?

Schematics / Symbols

- Implement such an oscillator
  - Use global power nets vddd! and gndd! and substrate gnd! (symbols from analogLib)
  - Use transistors N_18_MM and P_18_MM from the technology library UMC_18_CMOS
- Create 3 schematics with corresponding symbols:
  - Inverter
    - use pins **in, out**
    - use an NMOS with W/L = 0.5u/0.18u and a 3 times wider PMOS
  - NAND2
    - use pins **in1, in2, out**
    - use MOS such that the drive strength is roughly as for the inverter
  - Oscillator
    - use pins **run, out**
    - use (for instance) 10 inverters
    - use a **compact notation**, i.e. do NOT draw 10 inverters

Hint

- To make the schematic compact, and to prepare for very long inverter chains, instantiate N inverters in one step:
  - Inv<9:0> (for N=10)
- Label the nets correspondingly.

Simulation

- Create another schematic SIM_RingOsc for simulation
- Instantiate
  - the oscillator
  - the power supply source (of 1.8 V)
  - a vpulse source to turn on the oscillator after 5 ns.
- Connect gnd! and gndd! with a 0V voltage source

- Does it oscillate ? What is the oscillation frequency ?
  - (Use pins 'a' and 'b' in the waveform display)
- What follows for the delay of *one* inverter (neglecting NAND2)

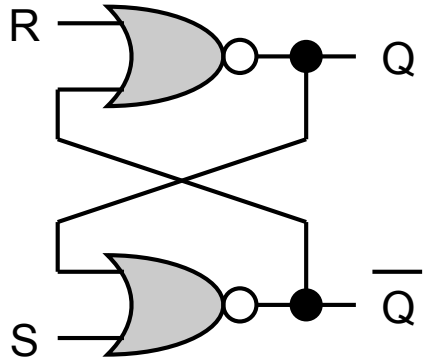
- Change your circuit to N=50 or so and repeat.

- Such circuits are often used to easily measure the very small delay of an inverter or other cells

EXERCISE B: SET-RESET FLIPFLOP

Creating the Cells

- A Set-Reset Flipflop (SF-FF) can be implemented by the following schematic

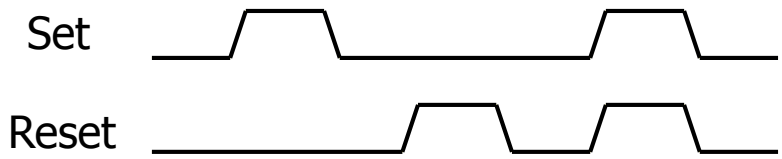


- Create Schematic and Symbol of a NOR2
  - Use global nets vddd!, gndd! and gnd! for supply / ground / bulk
  - Use two input pins I0, I1 and one output pin Q
  - Use minimum size NMOS (N_18_MM) and PMOS (P_18_MM) from the UMC library UMC_18_CMOS

- Create Schematic and Symbol of the SF-FF
  - Use pin names as shown above

Simulation

- Create a simulation schematic and simulate the SR-FF
  - Do not forget the voltage supply source (use 1.8V)!
  - Add *vpulse* sources from *analogLib* to generate stimuli, for instance:



(the pulses should be a few Nanoseconds long)

  - Is everything as expected?
  - What is the delay between inputs and Q and !Q?
  - What happens if Set=Reset=1?

  - Add 1pF capacitive loads to the outputs and see what happens!